

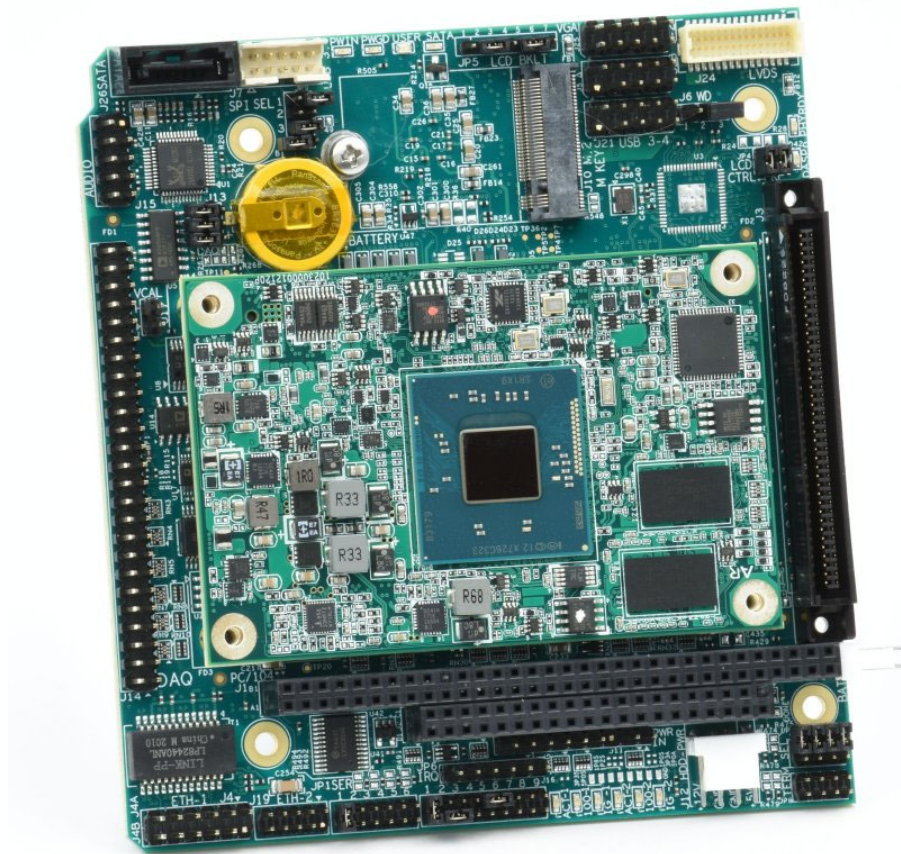


Athena IV

COM Express PC/104 SBC with Integrated Data Acquisition

User Manual

Revision 2.66



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Notices

Technical Support

Please use the [Technical Support Request](#) form to request assistance with a product you have already purchased.

Product and Sales Inquiry

Please use the [Sales Inquiry](#) form to request assistance with selecting a product for your application, or to obtain further information about products and service.

Limited Warranty

Diamond Systems Corporation provides a Limited Warranty for all items in this guide that it manufactures and sells, pursuant to terms provided in the [Diamond Systems Corporation Limited Warranty](#). No other warranty, express or implied, is included. Please download the warranty for additional information.

Trademarks

All trademarks, logos and brand names are the property of their respective owners.

Important Safe Handling Information

	WARNING! ESD-Sensitive Electronic Equipment • Observe ESD-safe handling procedures when working with this product. • Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories. • Always store this product in ESD-protective packaging when not in use.
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Safe Handling Precautions

The Athena IV carrier board contains a high number of I/O connectors with connections to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation, and connection to other equipment.

This section provides critical, best practice suggestions to avoid damage to your products. It includes descriptions of many common causes of damage – all of which can void your warranty.

Please follow these guidelines to be aware of common causes of damage and take the necessary precautions to prevent damage to your Diamond Systems' (or any vendor's) embedded computer boards.

Damage from incorrect handling or storage

- Physical and electronic damage can occur from mishandling. The following are frequent scenarios.
- An electrostatic discharge (ESD) causes a board to malfunction or stop working entirely. If ESD occurs, typically there is no visual sign of damage. While it is often difficult to identify faulty component(s), if the fault is identified there is a good chance that the board can be repaired.
- A screwdriver slips during installation, causing a gouge in the PCB surface and cutting signal traces or damaging components.
- A board is dropped, causing damage to the circuitry near the point of impact. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge. These design rules can minimize but cannot always prevent damage from impact.
- A short occurs when a metal screwdriver tip slips, or a screw drops onto a board while it is powered on. This can cause overvoltage or power supply problems described below.
- A storage rack with slots to hold boards can damage components near the board edge. Many boards have components that are close to the board edge, which are subject to damage in racks.
- Connector pins are bent by improperly dis-assembling attached boards or ribbon cables from a pin header, or from physical impact or improper storage. Typically, bent pins can be repaired one at a time with needle-nose pliers. Severely bent or frequently repaired pins may require the replacement of the connector.

Best Practices to avoid damage during handling or storage

- To prevent ESD damage, always follow proper ESD-prevention practices when handling any electronic components.
- To prevent physical damage from impact, handle all boards with care and work in a safe, spacious environment.
- To prevent short circuit damage from a metallic tool or dropped screw, perform assembly operations ONLY when the system is powered off.

- To prevent damage to fragile components and connector pins in storage, always store boards in individual ESD-safe sleeves in sturdy bins with dividers between boards. Do NOT use racks with slots, or stack boards in a pile or in close proximity.
- To prevent damage to connector pins during assembly or dis-assembly, use caution to align connectors and especially when force is needed to disassemble components and wires. Do not 'rock' connectors back and forth or pull any component at the wrong angle.

Damage due to incorrect voltage or connections

Power supply wired backwards

Diamond Systems power supplies and boards are not designed to withstand a reverse power supply connection. Reverse power will destroy nearly every IC that is connected to the power supply. Reverse power damage is rarely repairable. Check twice before applying power!

Board not installed properly in PC/104 stack

If a PC/104 board is accidentally shifted by 1 row or 1 column (of pins) it is possible for power and ground signals on the bus to contact the wrong pins. For example, this can damage components attached to the data bus because it puts the $\pm 12V$ power supply lines directly on data bus lines.

Overvoltage on analog input

If a voltage applied to an analog input exceeds the design specification of the board, the input multiplexor and/or parts behind it can be damaged. Most of our boards will withstand an erroneous connection of up to $\pm 35V$ on the analog inputs, even when the board is powered off, but not all boards, and not in all conditions.

Overvoltage on analog output

If an analog output is accidentally connected to another output signal or a power supply voltage, the output can be damaged. On most of our boards, a short circuit to ground on an analog output will not cause trouble.

Overvoltage on digital I/O line

If a digital I/O signal is connected to a voltage above the maximum specified voltage, the digital circuitry can be damaged. On most of our boards the acceptable range of voltages connected to digital I/O signals is 0-5V, and they can withstand about 0.5V beyond that (-0.5 to 5.5V) before being damaged. However, logic signals at 12V and even 24V are common, and if one of these is connected to a 5V logic chip, the chip will be damaged, and damage may extend past that chip to others in the circuit.

Best Practices to avoid damage due to incorrect voltage or connections

- Ensure all power supply connections are correct and not reversed!
- Ensure all pins are aligned properly before and after assembling boards and components!
- Ensure proper voltage is supplied to all analog inputs!
- Ensure all analog voltage outputs do not connect to another signal output or power supply output!
- Ensure all voltages for digital I/O lines are proper and within range, and that higher voltage signals (24V or 12V) are not supplied to lower voltage circuits (12V or 5V)!

IMPORTANT! Always check twice before Powering Up!

1. Introduction

1.1. Athena IV Product Overview

The Athena IV carrier board is the fourth generation in the Athena family of rugged, wide-temperature PC/104 SBCs (Single Board Computers) with (optional) integrated data acquisition.

The Athena IV is designed as a replacement product for the Athena II and III, featuring physical conformance to the earlier models to enable fast and easy upgrades. Athena IV is an excellent choice for:

- Customers who are using previous generations of Athena seeking to extend the lifetime of their existing product
- Customers who are seeking to replace an obsolete PC/104 SBC with a newer generation SBC to extend their existing product's lifetime
- Customers seeking to build a PC/104 system expected to have a long service lifetime.

1.2. COM Architecture

Athena IV is a COM (Computer-on-Module) carrier that uses COM Express Mini type 10 modules to provide CPU functionality. The board maintains the PC/104 stack through the same ISA bus used on the Athena II and III.

The use of a COM-based architecture yields many significant benefits over a true single-board computer where the processor and related circuitry are included on the main board:

- **Scalable CPU performance** - you can swap out one COM for another in the exact same form factor but with a different CPU. This allows your system to be easily upgraded when software demands increase, while avoiding any mechanical redesign.
- **Extended product lifetime** - if the COM you're using becomes obsolete, another one can be used in its place easily, with no mechanical changes required to the system. This enables COM-based embedded systems to easily last 20 years, since most of the baseboard electronics usually have much longer lifecycles than the processor and related peripherals contained on the COM.
- **Higher feature density / smaller overall size** - A 2-board solution provides twice the PCB area in the given footprint, allowing more circuitry and more features to be included.
- **Earlier access to the latest CPU technology** - Most new processors are introduced in COMs long before they are available in true single-board computer form. With a COM-based SBC you can upgrade your system with the latest CPU sooner, again without having to engage in any mechanical redesign.
- **Consistent platform across product lines** - the CPU scalability and interchangeability mean that a single physical form factor can be used in multiple applications requiring different CPU capabilities.

1.3. COM Processor Options

Athena IV accepts COM Express Type 10 Mini modules. The processor, system memory and onboard eMMC capacity are determined by the module installed, so the exact feature set of a given Athena IV depends on the COM fitted. Athena IV currently ships with the following Intel Apollo Lake modules. Contact Diamond Systems for availability of additional options.

<i>CPU</i>	<i>Features</i>
E3940	Apollo Lake, quad core, 1.6GHz, 8GB RAM, 64GB eMMC
E3950	Apollo Lake, quad core, 8GB RAM, 128GB eMMC

1.4. Physical Configuration

The Athena IV carrier board is approximately 4.175" x 4.475" with various cutouts in the corners. The carrier board is the base layer in the stack. The COM Express module mounts on the top side of the carrier board, along with PCIe104 expansion sockets. A heat sink sits above the carrier board and COM Express module, providing efficient cooling to the system.

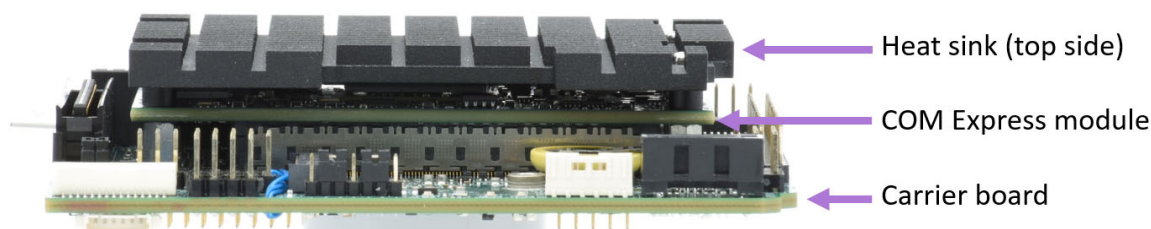


Figure 1-1: Athena IV configuration with COM Express module and Heat Sink

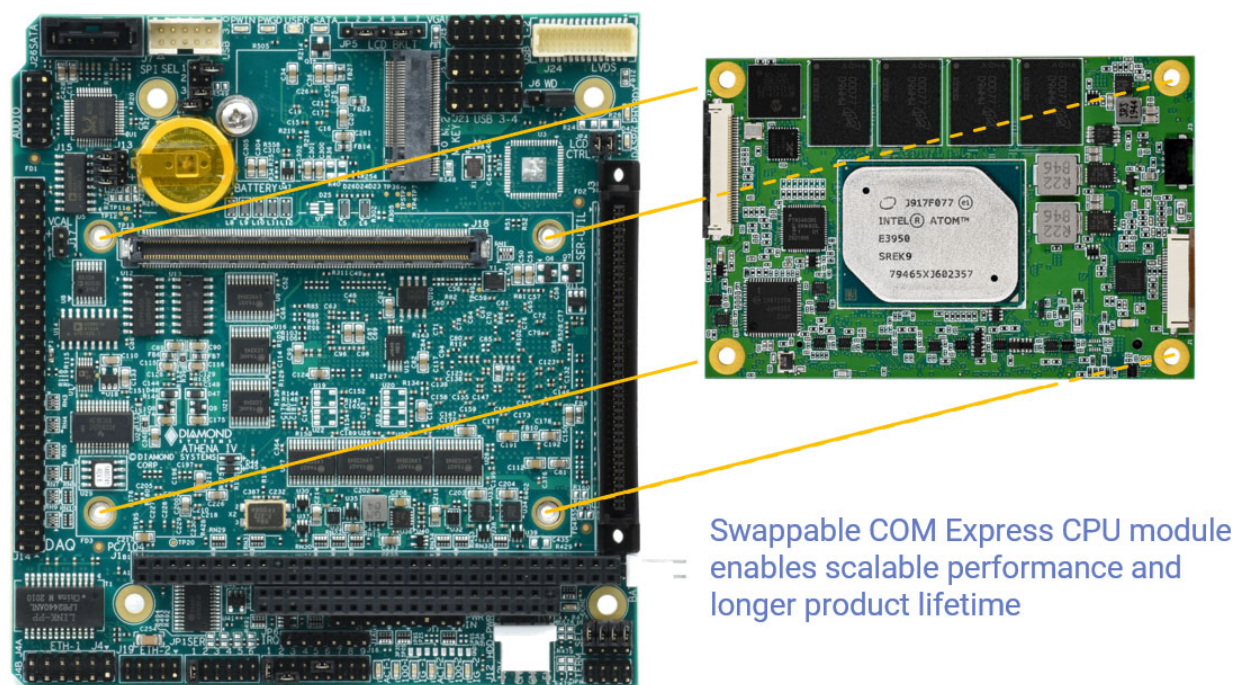


Figure 1-2: Athena IV carrier board with COM Express module placement

1.5. Comparison to Athena II and Athena III

Due to advances in technology, not all features of Athena II and Athena III can be carried forward to the Athena IV. The following table highlights key component and design differences.

Note: The table provides specifications for the CMN-E3940 or CMN-E3950 COM installed, however other COMs can be used to provide different processor and RAM capabilities.

Feature	Athena II	Athena III	Athena IV
Processor	VIA Mark 533/800MHz	Intel E640T/E680T Tunnel Creek	COM Express Type 10 with Intel Apollo Lake E3940 or E3950
RAM	256MB soldered	1GB soldered	8GB soldered on COM
Mass storage	IDE	USB flash disk up to 8GB	M.2 2230 M-Key SATA SSD; 64GB or 128GB eMMC on COM
Ethernet	10/100 port on 1x6 0.1" pin header	10/100/1000 port on 2x5 2mm pin header	10/100/1000 port, connector 2x6 2.54mm pin header 2 nd Port via PCIe to Ethernet (I210) on 2x5 2mm pin header
Serial ports	2 RS-232 from chipset, 2 RS-232/485 from 16C2850 UART	4 RS-232/422/485, BIOS configuration; 2 from super I/O, 2 from 16C2850 UART	4 RS-232/422/485, jumper configuration; from XR17V354 PCIe quad UART; 2 serial ports are multiplexed between XR17V354 & XR16C2850
USB Ports	4x USB2.0ports terminated with 2x5 2.54 mm pitch header	4x USB2.0 ports terminated with 2x5, 2.54mm pitch header& 1 port used for on-board USB flash disk	4x USB2.0 ports terminated with 2x5 2.54mm pitch header & 1 USB3.0 port terminated with 2x5 10 pin vertical connector
Audio	Via VT1612A Audio CODEC available on 2x5 2.54mm pin header	Via ALC262 Audio CODEC available on 2x5 2.54mm pin header	Via ALC262 Audio CODEC available on 2x5 pin header
Display VGA	Processor Output on 2x5 2.54mm pin header	SDVO to RGB converter CH7317B available on 2x5 2.54mm pin header	Via DDI to VGA converterCH7517 available on 2x5 2.54mm pin header
Display LVDS	Provided by processor available on 2x15 header	Provided by processor available on 2x15 header	From COM module, available on 2x15 header
Parallel port	1 from chipset	1 from super I/O	NA
PS/2	Keyboard / mouse from chipset	Keyboard / mouse from super I/O	NA
CD	Analog CD input	NA	NA
ISA bus	Provided by processor	Provided via 85226 LPC to ISA bridge	Provided via LPC to ISA core within Artix 7 FPGA

1.6. Athena IV Ordering Guide

1.6.1. Available Models

<i>Product Number</i>	<i>Product</i>
ATH4-E3940-8G064A	Athena IV SBC, E3940 1.6GHz Quad Core CPU, 8GB RAM, With DAQ
ATH4-E3940-8G064N	Athena IV SBC, E3940 CPU, 8GB RAM, 64GB eMMC, With DIO
ATH4-E3950-8G128A	Athena IV SBC, E3950 CPU, 8GB RAM, 128GB eMMC, With DAQ
ATH4-E3950-8G128N	Athena IV SBC, E3950 CPU, 8GB RAM, 128GB eMMC, With DIO
ATH4-BB01A	Athena IV Baseboard, with DAQ
ATH4-BB01N	Athena IV Baseboard, without DAQ

1.6.2. Development kits

Includes SBC, software SDK, and cable kit.

Development kits are available to support quick project startup. Each kit includes the Athena SBC, a cable kit, and a programmed 64GB flashdisk with your choice of Windows 10 or Linux operating system, ready to run. Simply plug in the flashdisk, attach the cables, add your keyboard, mouse, and display, and you're ready to boot into a fully functional OS. Configuration files and instructions are provided to rebuild the OS with your application. The Linux kit includes all the tools needed to rebuild the OS. The Windows 10 kit includes a runtime license.

<i>Product Number</i>	<i>Product</i>
DK-ATH4-E3940-8G064A-LNX64	Dev Kit, Athena IV SBC, E3940 CPU, 64GB eMMC, Linux 64-bit OS
DK-ATH4-E3940-8G064A-WE1064	Dev Kit, Athena IV SBC, E3940 CPU, 64GB eMMC, Windows 10 64-bit OS
DK-ATH4-E3950-8G128A-LNX64	Dev Kit, Athena IV SBC, E3950 CPU, 64GB eMMC, Linux 64-bit OS
DK-ATH4-E3950-8G128A-WE1064	Dev Kit, Athena IV SBC, E3950 CPU, 64GB eMMC, Windows 10 64-bit OS

1.6.3. Software development kits

Pre-configured OS on a flashdisk with backup USB memory stick.

<i>Product Number</i>	<i>Product</i>
SDK-ATH4-E3940-8G064A-LNX64	Software Dev Kit, Athena IV SBC, E3940 CPU, 64GB eMMC, Linux 64-bit OS
SDK-ATH4-E3940-8G064A-WE1064	Software Dev Kit, Athena IV SBC, E3940 CPU, 64GB eMMC, Windows 10 64-bit OS
SDK-ATH4-E3950-8G128A-LNX64	Software Dev Kit, Athena IV SBC, E3950 CPU, 64GB eMMC, Linux 64-bit OS
SDK-ATH4-E3950-8G128A-WE1064	Software Dev Kit, Athena IV SBC, E3950 CPU, 64GB eMMC, Windows 10 64-bit OS

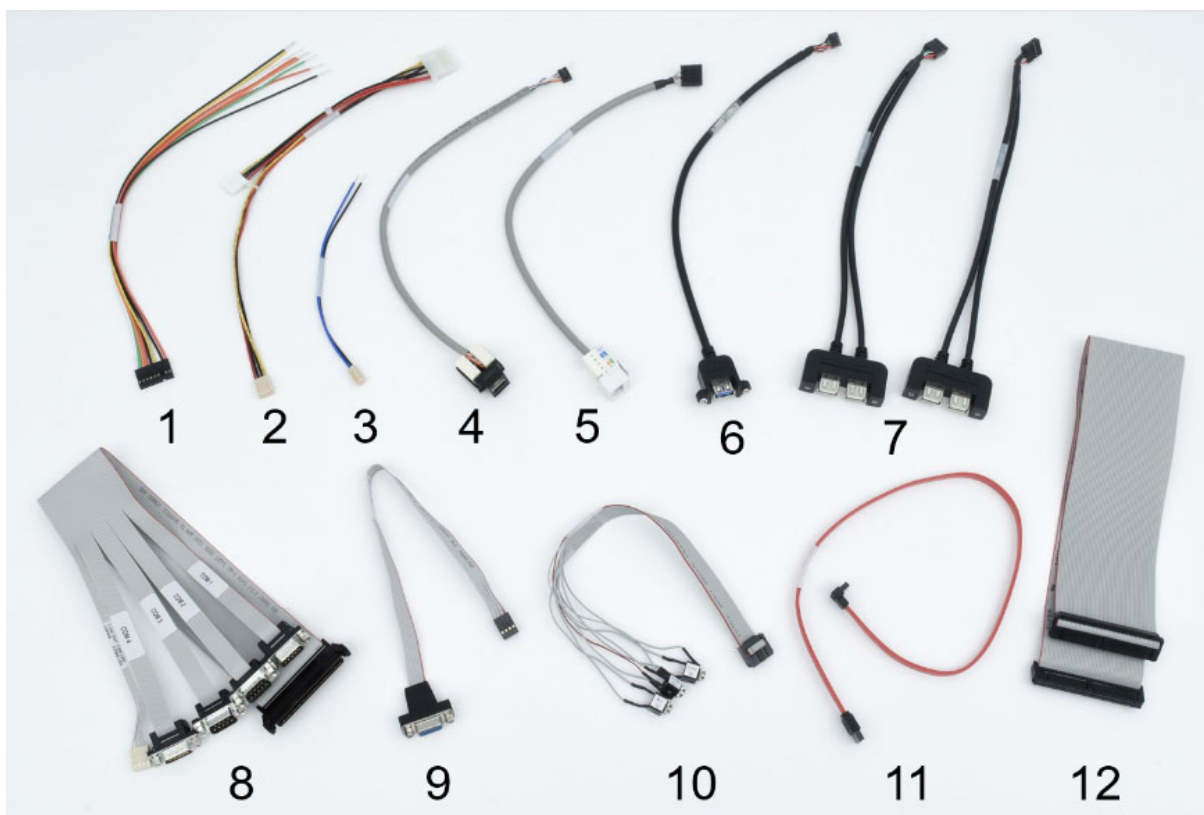
1.6.4. Cable kits

The Athena IV cable kit is ordered as CK-ATH4-01. It contains the cables listed below.

Athena IV is designed to use most of the same cables as previous generations of Athena, along with upgrades for the latest technology. New with Athena IV is a second gigabit Ethernet port which is backwards compatible with the original board's 10/100 connector along with a USB 3.0 cable.

Cables are normally sold as complete kits. Individual cables may be available in some cases or may be ordered with minimum order quantities; contact us for details.

Item	Part Number	Description
	CK-ATH4-01	Athena IV cable kit (includes all items numbered 1 to 12)
1	6981009	Cable, Power I/O, Stranded x9 to Trim wires x9, 12"L
2	6981006	Cable, Power Out, 4 pos Female to 22013047 4 pos and 22013067 IDC Skt 4 pos
3	6981011	Cable, Panel Input / External Battery, 770602-2 2 pos to stranded wire 2 pos, 6"L
4	6981080	Gigabit Ethernet cable, RJ-45 socket, 10 pin board connector
5	6981086	Gigabit Ethernet cable, RJ-45 socket, 12 pin board connector
6	6980603	Cable, FCI 2x5 2mm latching to USB 3.0 type A panel mount
7	6981012	Cable, USB, 10-Pin Hdr to Dual USB skt w/ pnl mt inserts, 12"L
8	6981014	Cable Assy, 80 Pin Socket, 2x20 to 4x Serial DB9M
9	6981030	Cable, VGA, 2x4 .1" to DB15F HD, 12"L Ribbon
10	6981031	Cable, Audio, 2x5 .1" IDC F to x3 3.5mm Jack, 12"L Ribbon
11	6989101	SATA Cable, 7-Pin Data, Straight to Right Angle, 500mm
12	C-50-18	50-conductor .1" pitch 18" ribbon cable



1.7. Product Photos

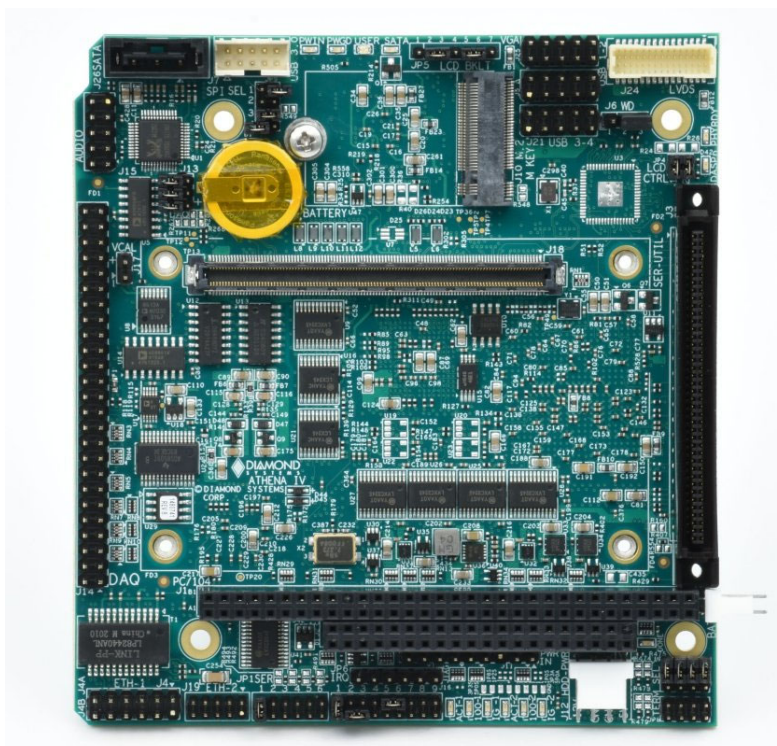


Figure 1-3: Athena IV carrier board, top side

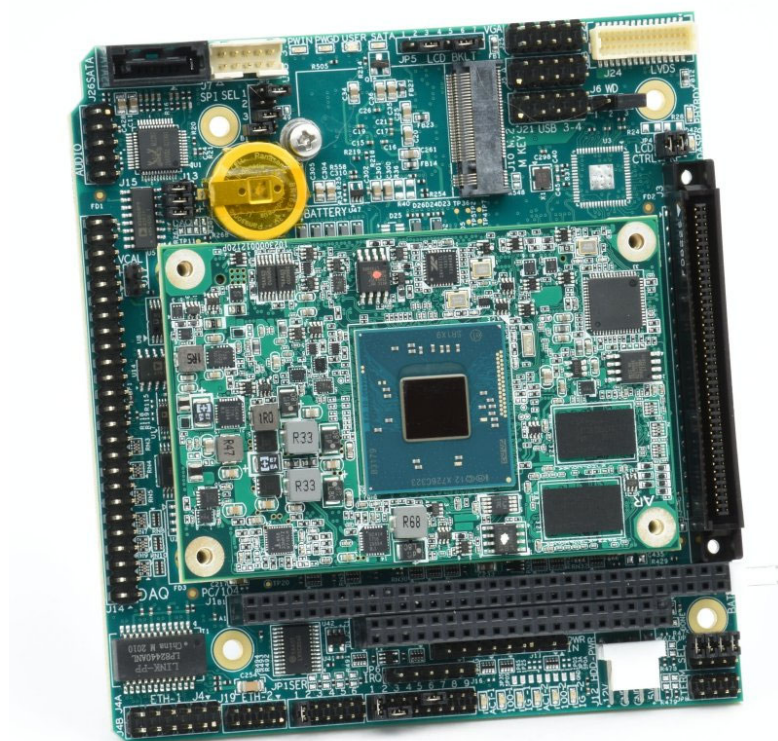


Figure 1-4: Athena IV carrier board, top side with COM Express module installed

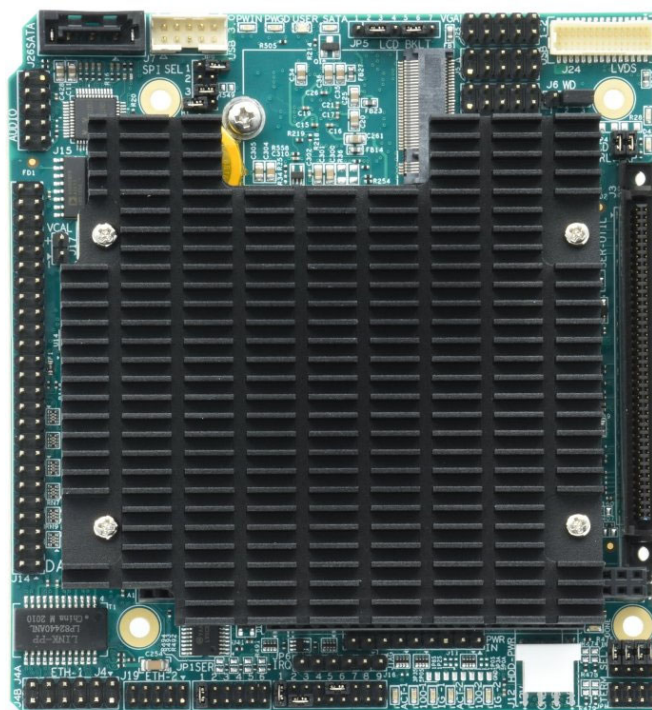
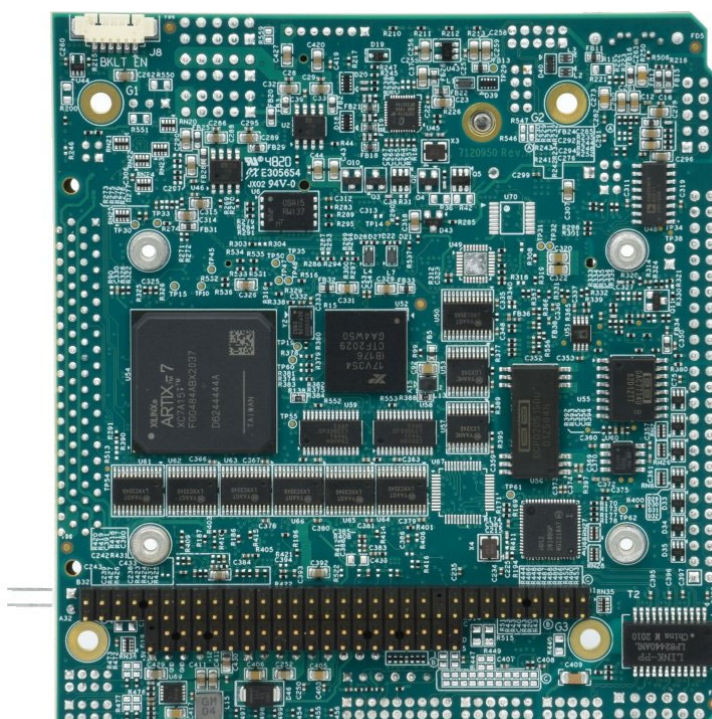


Figure 1-5: Athena IV, top side with heat sink installed



2. Feature List

- COM-based architecture for long product life and performance scalability
- Integrated professional quality data acquisition circuit saves space
- Downward stacking PC/104 ISA bus connector supports a wide range of I/O modules for easy system I/O expansion
- M.2 2230 SATA socket supports up to 128GB flashdisk
- Form factor and most connectors backwards compatible with previous generations of Athena for easy product migration
- Heat sink cooling
- 5VDC input voltage
- 4.175 x 4.475" / 106 x 114mm W x H
- -40/+85°C operation fanless
- Windows 10 and Ubuntu Linux OS support

2.1. SBC Features

- Choice of E3940 or E3950 Atom CPU
- 8GB RAM soldered on COM
- 2 gigabit Ethernet ports
- VGA + Single-channel 24-bit LVDS
- 1 USB 3.0 port + 4 USB 2.0 ports
- 4 RS-232/422/485 serial ports with dual software/jumper configuration control
- HDA audio (ALC262)
- 7-pin SATA connector plus M.2 2230 socket
- On-board RTC backup battery plus external battery connector

2.2. Data Acquisition Subsystem Features

- 16 single-ended / 8 differential analog inputs
- 16-bit A/D resolution
- Unipolar and bipolar analog inputs
- Single-ended and differential input configuration
- Programmable gain 1/2/4/8 providing input ranges +/-10V / 0-10V down to +/- 1.25V / 0-1.25V
- 150KHz maximum A/D sample rate, single-channel and multi-channel mode
- Internal clock / external clock / software A/D triggering
- Single-channel and multi-channel-scan A/D operation
- Interrupts with FIFO to support reliable high-speed sampling
- 4 12-bit single-ended analog outputs
- +/-10V, +/-5V, 0-10V and 0-5V output ranges
- Autocalibration with Universal Driver software maintains accuracy over time and temperature
- 24 digital I/O, 3.3V logic / 5V tolerant inputs
- 2 programmable counter/timers for A/D timing and general counting purposes
- Up to 128GB eMMC Flash integrated onto COM

2.3. Athena IV Carrier Board Feature List

Feature	Description	Connector Type
Power	+5V DC input supply +12V, -12V, -5V DC to pass through to expansion buses and LCD backlight ONLY.	TH ST 9POS 2.54mm
HDD Power Output	+5V DC output supply +12V DC output supply	TH-RA 4POS 2.54mm
External Battery	External Battery connector for RTC	TH RA 2 POS 2.54mm
Mass storage	1 M.2 socket	RA M.2 connector 67 Position
	SATA Port	Standard 7 position port
USB	4x USB 2.0	2x5 Header 2.54mm - 2 Nos.
	1x USB3.0	2x5 vertical connector 2mm
Ethernet	ETH1- 10/100/1000Mbps from COM module	2x6 Header 2.54mm
	ETH-2-10/100/1000Mbps via I210 Ethernet controller	2x5 Header 2mm
Serial ports	4 ports through XR17V354. 2 ports multiplexed with XR16C2850 for backward compatibility Jumper configurable RS-232/422/485 through SP336 transceivers	80 Pin High density connector
Audio	HDA to Analog Audio converter (ALC262)	2x5 Header 2.54mm
Display	VGA through DDI to VGA converter (CH7517)	2x5 Header 2.54mm
	1 x Single Channel 24-bit LVDS port	2x 15 Header SMT
LCD Backlight	LCD backlight power and control signals	1x6 Header SMT
Analog IOs	Analog Inputs - 16 SE or 8 Diff through ADS8509 Software programmable SE/DI, +/-10V, +/-5V, +/-2.5V, +/-1.25V, 0-10V, 0-5V, 0-2.5V	2x25 Header
	Analog Outputs - 4 outputs through DAC7714UB Software programmable range +/-10V, +/-5V, 0-10V and 0-5V range	
Digital IOs	24 programmable digital I/O, 3.3V logic O/P and 5V I/P tolerant I/Os Configurable as PWM and Counter outputs	

Operating System Support

Windows 10 and Linux

Physical

Form-Factor	106mm x 114 mm / 4.175" x 4.475"
Cooling Mechanism	Heat sink, fanless
Power Input Range	+5V DC +/-5%
Operating Temperature Range	-40°C to +85°C ambient (final system specification depends on the COM installed)

3. Block Diagram

The following diagram illustrates the key functional blocks of the Athena IV COM Express Carrier board.

Note: The diagram shows all available features. The exact implemented features depends on the installed COM.

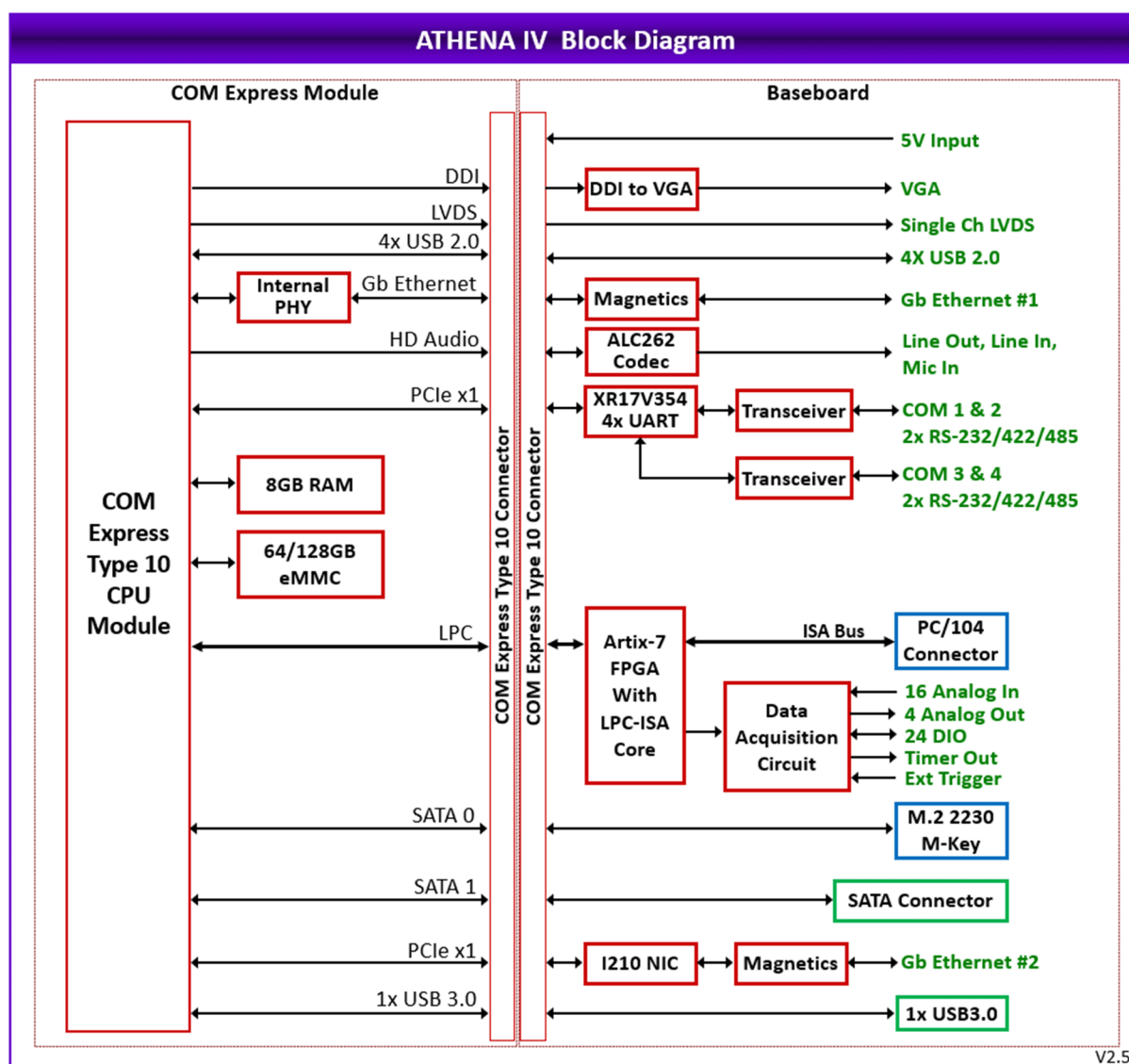


Figure 3-1: Athena IV COM Express Carrier Board Block Diagram

4. Functional Overview

This section provides functional details of the key subsystems implemented on Athena IV.

4.1. COM Express Carrier Board

Athena IV is a two-board solution consisting of a carrier board with an installed Computer-on-Module (COM) and thermal solution. Athena accepts COM Express Type 10 modules. As of this version of this manual, the board currently ships with Intel Apollo Lake E3940 and E3950 processor modules. The availability of features is module dependent. Contact Diamond Systems for information on additional COM options.

4.2. Power Supply Specifications

The board requires +5VDC +/-5% for operation. The on-board power supply circuit supports the following loads on the various features.

In addition, a pin is available to attach +12 VDC, however this voltage is routed only to the LCD backlight connector and the PC/104 expansion bus connectors. No on-board circuit connects to +12V. The board is provided with ACPI power pushbutton for on/off control.

5V	3.3V	Feature
	0.5A	M.2
2A		USB 2.0 Ports
1A		USB 3.0 Port
3A		COM Express Module

4.3. Backup Battery

A 2pin connector is provided for connecting the external backup battery.

An onboard BR1632/HFN 120mAh coin cell battery maintains the system real-time clock. A 1x2 connector (J9) is also provided to enable the use of an external battery.

4.4. Ethernet Ports

The board provides two 10/100/1000 Ethernet ports. The first port comes directly from the COM module. The second port is derived from the Intel WGI210IT PCIe Ethernet controller. The first port is terminated with a 2x6 2.54mm pin header. The left column of the 2x6 pin header maintains backward compatibility with the Athena II Ethernet connector. 2nd Ethernet port is available on a 2x5 pin header that matches later generation Diamond Systems SBC Ethernet ports.

On-board LEDs are provided for Link, Activity, and Speed on each port. The LEDs are located along the board edge near the Ethernet connectors. Both connectors do not provide access to the LED signals.

4.5. PC/104

The PC/104 expansion bus enables installation of additional I/O boards. It consists of two stack-through connectors press-fit onto the board. The PC/104 connectors support stack-down only due to the heat sink covering the top side sockets. The PC104 bus operates with 5V logic levels. The 5V supply on the PC/104 connector is routed directly to the input power connector, so that the board may obtain its input power from either the input power connector or the PC/104 bus connectors. PCB key pins B10 and C19 are marked with square pads visible on the bottom side. Pins B10 and C19 are plugged with inserts. PC/104 connectors are identified as J1 (64-pin 8-bit connector) and J2 (40-pin 16-bit connector). The ISA bus is realized using LPC to ISA IP core within an Artix 7 FPGA.

4.6. PCIe Link Routing

3 PCIe lanes from the COM are utilized in the carrier card.

- Lane 1 – PCIe to UART
- Lane 2 – Second Gigabit Ethernet through i210 Ethernet controller
- Lane 3 – PCIe to FPGA for future use

4.7. USB

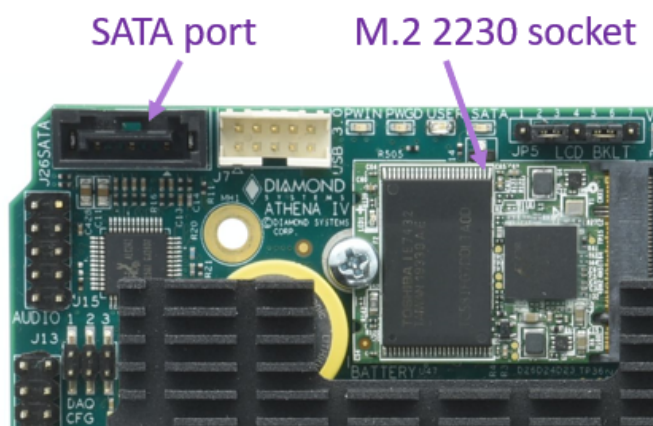
Carrier card utilizes 4x USB2.0& 1x USB3.0 ports from the COM.4 x USB2.0 ports are routed to 2x5 headers. USB3.0 signal is routed to a 2x5 vertical connector.

4.8. SATA

The board supports 2 SATA ports.

One SATA port is connected to an M.2 SATA connector for onboard mass storage. The M-Key connector supports a 2230 M.2 card. Modules up to 128GB are available.

The second SATA port is routed to a standard 7-pin SATA connector for an external drive. Diamond Systems offers accessory board ACC-HDDMOUNT, which allows a 2.5" drive to be mounted on the PC/104 stack. This connector does not support SATA-DOM.



4.9. Audio

HD audio link available in the COM module is converted to Analog Audio using Audio codec ALC262. Line In, Line OUT and Mic In signals are terminated with a 2x5 header.

4.10. Video

VGA

The board supports VGA display interface. On board DDI to VGA chip(CH7517) is used to convert the DDI interface from COM module. Maximum VGA resolution supported is 2048x1152@60Hz

LVDS LCD

Athena IV supports a 24-bit single channel LVDS display through 2x15Vertical latching connector. Separate backlight supply connector provides LCD backlight supply and PWM control. Backlight supply is given externally through the main power input connector.

4.11. Serial Ports

The board supports 4 serial ports using PCIe to Quad UART controller (XR17V354). The UARTs built into the COM are not utilized. All the 4 ports support RS232/422/485 configuration realized using SP336 transceivers. Protocol selection for Serial ports 1-4 and Termination (121 Ohm) for RS422 and RS485 protocols are selected using jumpers.

4.12. Data Acquisition

The board provides a data acquisition sub circuit containing analog input, analog output, and digital I/O features. This circuit is controlled by an FPGA attached to the COM module via the LPC bus. A pin header on the board provides access to JTAG signals for reprogramming the FPGA on the board and in the field.

The data acquisition circuit identical to that found on the Diamond Athena I / II / III board.

Features of the DAQ include:

- 16 single-ended / 8 differential analog inputs with 16-bit resolution, programmable input ranges, and 200KHz sample rate;
- 4 analog outputs with 16-bit resolution and programmable output ranges
- 24 digital I/O in 3 8-bit ports with programmable direction, buffered outputs, and configurable pull-up/down resistors
- 1 External trigger Input and 1 Timer Output.

4.13. LED Indicators

The board provides the following LED indicators. All LEDs are located near the board edges and labeled in silkscreen with their function.

<i>Function</i>	<i>LED color and operation</i>	<i>PCB label</i>	<i>Location</i>
Power in:	Green LED for 5V	PWIN	Top
Power Good	Green LED for Power Good indication.	PWGD	Top
Ethernet:	Green LED for Link, activity, and speed for each port	ACT / 100 / 1G	Bottom
SATA ACT#	Green LED for SATA activity	SATA	Top
FPGA DONE:	Green LED for FPGA_DONE	DONE	Lower right PC104 hole
User LED:	Blue LED driven by data acquisition FPGA	USER	Top

4.14. Trusted Platform Module

The board provides an optional Board ID security solution from Infineon using the SLB9670XQ12FW643XUMA1. SLB9670XQ12FW643XUMA1 is interfaced to the COM over SPI interface.

5. Data Acquisition Circuit

Athena IV is available in two configurations, with & without data acquisition. An integrated professional-quality data acquisition circuit features analog and digital I/O with full programming library support. The data acquisition circuit is identical to the one used on Athena II. (HOW ABOUT ATHENA III?)

Athena IV belongs to Diamond's 2-in-1 series of SBCs with integrated data acquisition. For applications requiring precision analog I/O, a 2-in-1 SBC is an ideal choice because it reduces the number of boards in the system, resulting in a system that is smaller, lighter, lower cost, and easier to assemble and maintain.

The data acquisition circuit on Athena IV includes the following:

- 16 channels of 16-bit A/D, 4 channels of 12-bit D/A, and 24 channels of digital I/O.
- Analog inputs feature single-ended and differential configuration, programmable input ranges, and fault-protected channel multiplexors to protect against overvoltages.
- D/A channels feature programmable output ranges and simultaneous update capability.
- Both A/D and D/A circuits include Diamond's advanced auto-calibration technology, enabling the board to be quickly calibrated in software without the use of trim pots that are subject to tampering, mis-adjustment, or shock and vibration.
- A/D and D/A circuits feature lower noise, higher bandwidth, and more configuration flexibility than competing analog I/O circuits.

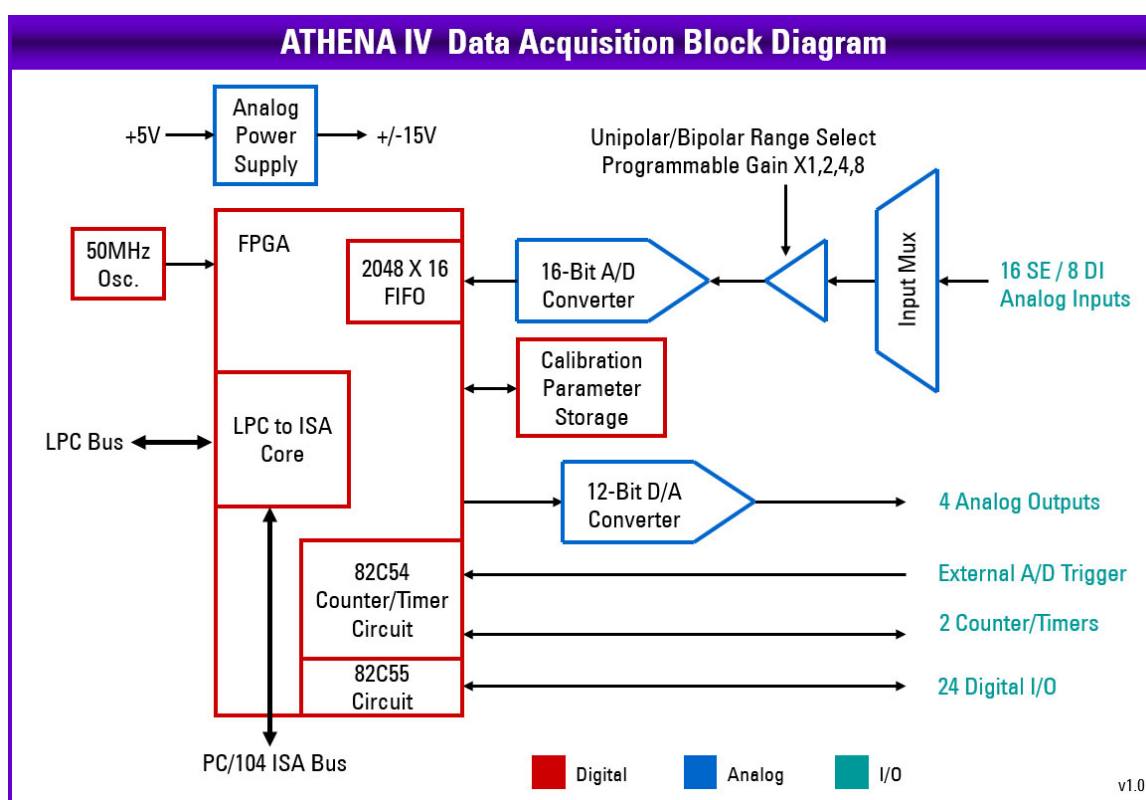


Figure 5-1: Athena IV data acquisition block diagram

5.1. Data Acquisition Circuitry I/O Map

5.1.1. Overview

The data acquisition circuitry on Athena IV occupies 16 bytes in I/O memory space. The default address range is 280h (base address) to 28Fh.

5.1.2. Register Map Page Summary

The following table summarizes the DAC register functions. The registers are paged to allow access to enhanced functions. There are three register pages and the desired page is selected using the A/D gain and scan settings register, Base+3, bits PG0-PG1, provided the board is in enhanced mode.

Base +	Write Function	Read Function
DAQ Main Registers		
0	Command	A/D LSB (bits 7-0)
1	Enhanced Mode Control/Page setting	A/D MSB (bits 15-8)
2	A/D Scan Channel	A/D Scan Channel L/H Read-back
3	A/D Gain and Scan Settings / Page Control	A/D-D/A Gain and Status Read-back
4	Interrupt / Counter Control	Interrupt / Counter Control Read-back
5	FIFO Threshold	FIFO Threshold Read-back
6	D/A LSB	FIFO Current Depth / FIFO Status
7	D/A MSB / DAC Channel	Interrupt and A/D Channel Read-back
8	Digital I/O Port A Output	Digital I/O Port A Input
9	Digital I/O Port B Output	Digital I/O Port B Input
10	Digital I/O Port C Output	Digital I/O Port C Input
11	Digital I/O / DA Control	Digital I/O / DA Control Read-back
DAQ Registers Page 0: Counter/Timer Access		
12	Counter/Timer D7-0	Counter/Timer D7-0
13	Counter/Timer D15-8	Counter/Timer D15-8
14	Counter/Timer D23-16	Counter/Timer D23-16
15	Counter/Timer Control	FPGA Revision Code
DAQ Registers Page 1: AutoCal Control		
12	EEPROM/TrimDAC data latch	EEPROM/TrimDAC data read-back
13	EEPROM/TrimDAC address latch	EEPROM/TrimDAC address read-back
14	EEPROM/TrimDAC control register	EEPROM/TrimDAC status register
15	Special features unlock register0	Page 1 ID Read-back
DAQ Registers Page 2: Expanded FIFO and AD /DA Control		
12	Expanded FIFO depth register	Expanded FIFO depth read-back
13	AD Mode Control	AD Mode Control Read-back
14	A/D scan interval	A/D scan interval
15	DAQ LED, Serial Port Control Register	Page 2 ID Read back
DAQ Registers Page 3: FPGA / Board ID		
12	RESERVED	RESERVED
13	RESERVED	RESERVED
14	None, Read only	FPGA Minor ID Read-back
15	None, Read only	FPGA Major ID Read-back

NOTE: 1. Page 0, registers 0-11 are accessible when Page 1 or Page 2 are selected.

5.1.3. Register Map Bit Summary

Write Register Summary

Base +	7	6	5	4	3	2	1	0
Main Registers								
0	STARTAD	RSTBRD	RSTDA	RSTFIFO	CLRDMA	CLRT	CLRD	CLRA
1							PG1	PG0
2	H3	H2	H1	H0	L3	L2	L1	L0
3	-	-	PG1	PG0	-	SCANEN	ADG1	ADG0
4	CKSEL1	FRQSEL1	FRQSEL0	ADCLK	DMAEN	TINTE	DINTE	AINTE
5	- / FT10	- / FT09	FT5/ FT08	FT4/ FT07	FT3/ FT06	FT2/ FT05	FT1/ FT04	FT0/ FT03
6	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
7	DACH1	DACH0	-	-	DA11	DA10	DA9	DA8
8	A7	A6	A5	A4	A3	A2	A1	A0
9	B7	B6	B5	B4	B3	B2	B1	B0
10	C7	C6	C5	C4	C3	C2	C1	C0
11	DIOCTR		DASIM	DIRA	DIRCH	-	DIRB	DIRCL

Page 0: Counter/Timer Access

Base +	7	6	5	4	3	2	1	0
12	CtrD7	CtrD6	CtrD5	CtrD4	CtrD3	CtrD2	CtrD1	CtrD0
13	CtrD15	CtrD14	CtrD13	CtrD12	CtrD11	CtrD10	CtrD9	CtrD8
14	CtrD23	CtrD22	CtrD21	CtrD20	CtrD19	CtrD18	CtrD17	CtrD16
15	CTRNO	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

Page 1: AutoCal Control

Base +	7	6	5	4	3	2	1	0
12	D7	D6	D5	D4	D3	D2	D1	D0
13	A7	A6	A5	A4	A3	A2	A1	A0
14	EE_EN	EE_RW	RUNCAL	CALMUX	TDACEN	-	-	-
15	-- EEPROM Access Key Register --							

Page 2: Expanded FIFO and AD/DA Control

Base +	7	6	5	4	3	2	1	0
12	-	-	-	-	-	-	-	EXFIFO
13	-	-	DACPOLEN	DACPOL	ADPOL	ADPOLEN	ADSD	ADSDEN
14	-	-	-	-	-	-	-	SCANINT
15	DAQ_LED	-	-	SERCFG	SC3	SC2	SC1	SC0

Page 3: Board IDs

Base +	7	6	5	4	3	2	1	0
12	-	-	-	-	-	-	-	-
13	-	-	-	-	-	-	-	-
14	-	-	-	-	-	-	-	-
15	-	-	-	-	-	-	-	-

Read Register Summary

Main Registers

Base +	7	6	5	4	3	2	1	0
0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
2	H3	H2	H1	H0	L3	L2	L1	L0
3	ADBUSH	SE/DIFF	ADWAIT	DACBSY	OVF	SCANEN	ADG1	ADG0
4	CKSEL1	FRQSEL1	FRQSEL0	ADCLK	DMAEN	TINTE	DINTE	AINTE
5	- / FD07	- / FD06	FT5/FD05	FT4/FD04	FT3/FD03	FT2/FD02	FT1/FD01	FT0/FD00
6	FD7/FD11	FD6/FD10	FD5/FD09	FD4/FD08	FD3/OVF	FD2/FF	FD1/HF	FD0/EF
7	DMAINT	TINT	DINT	AINTE	ADCH3	ADCH2	ADCH1	ADCH0
8	A7	A6	A5	A4	A3	A2	A1	A0
9	B7	B6	B5	B4	B3	B2	B1	B0
10	C7	C6	C5	C4	C3	C2	C1	C0
11	DIOCTR		DASIM	DIRA	DIRCH	-	DIRB	DIRCL

Page 0: Counter/Timer Access

Base +	7	6	5	4	3	2	1	0
12	CtrD7	CtrD6	CtrD5	CtrD4	CtrD3	CtrD2	CtrD1	CtrD0
13	CtrD15	CtrD14	CtrD13	CtrD12	CtrD11	CtrD10	CtrD9	CtrD8
14	CtrD23	CtrD22	CtrD21	CtrD20	CtrD19	CtrD18	CtrD17	CtrD16
15	-- FPGA Revision Code --							

Page 1: AutoCal Control

Base +	7	6	5	4	3	2	1	0
12	D7	D6	D5	D4	D3	D2	D1	D0
13	A7	A6	A5	A4	A3	A2	A1	A0
14	-	TDBUSH	EEBUSH	CALMUX	-	-	-	-
15	-- 0xA1 --							

Page 2: Expanded FIFO and AD/DA Control

Base +	7	6	5	4	3	2	1	0
12	-	-	-	-	-	-	-	EXFIFO
13	-	-	DACPOLEN	DACPOL	ADPOL	ADPOLEN	ADSD	ADSDEN
14								SCANINT
15	-- 0xA2 --							

Page 3: Board IDs

Base +	7	6	5	4	3	2	1	0
12	-	-	-	-	-	-	-	-
13	-	-	-	-	-	-	-	-
14	0	0	0	0	0	0	0	1
15	0	0	0	1	0	1	1	0

5.1.4. Main Registers

Base + 0 Write Command Register

Bit No.	7	6	5	4	3	2	1	0
Name	STRTAD	RSTBRD	RSTDA	RSTFIFO	CLRDMA	CLRT	CLRD	CLRA
Reset	X	X	X	X	X	X	X	X

Base + 0 Read A/D LSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Reset	0	0	0	0	0	0	0	0

AD7 - 0 — A/D data bits 7 - 0; AD0 is the LSB; A/D data is an unsigned 16-bit value.

$$A/D \text{ value} = (\text{Base} + 0 \text{ value}) + (\text{Base} + 1 \text{ value}) * 256$$

Base + 1 Write Enhanced Features Access Register

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	PG1	PG0
Reset	0	0	0	0	0	0	0	0

Page Select (0 - 2): Accessible any time to select any of the 3 pages.

Base + 1 Read A/DMSB

Bit No.	7	6	5	4	3	2	1	0
Name	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Reset	0	0	0	0	0	0	0	0

AD15 - 8 — A/D data bits 15 – 8; AD15 is the MSB; A/D data is an unsigned 16-bit value.

Base + 2 Read/Write A/D Channel Register

Bit No.	7	6	5	4	3	2	1	0
Name	H3	H2	H1	H0	L3	L2	L1	L0
Reset	0	0	0	0	0	0	0	0

H3 – H0 High channel of channel scan range

L3 - L0 Low channel of channel scan range

Base + 3 Write Analog Input Gain / Page Control

Bit No.	7	6	5	4	3	2	1	0
Name	X	X	PG1	PG0	X	SCANEN	ADG1	ADG0
Reset	0	0	0	0	0	0	0	0

ADG1	ADG0	Gain	Unipolar Range	Bipolar Range
0	0	1	0-10V	±10V
0	1	2	0-5V	±5V
1	0	4	0-2.5V	±2.5V
1	1	8	0-1.25V	±1.25V

Base + 3 Read Analog Input Status

Bit No.	7	6	5	4	3	2	1	0
Name	ADBUSY	SE/DIFF	ADWAIT	DACBSY	OVF	SCANEN	ADG1	ADG0
Reset	0	1	0	0	0	0	0	0

ADBUSY A/D Busy. 1 = A/D conversion or scan in progress, 0 = A/D is idle.

SE/DIFF Single-ended / Differential mode indicator. 1 = Single Ended, 0 = Differential.

ADWAIT A/D input circuit status. 1 = A/D circuit is settling on a new value, 0 = ok to start conversion.

DACBSY Indicates the DAC is busy updating (approx. 30 µS). 1 = Busy, 0 = Idle.

OVF FIFO Overflow bit.

SCANEN Scan mode readback (see Base + 3 Write above).

ADG1-0 A/D gain setting readback (see Base + 3 Write above).

Base + 4 Read/Write Interrupt / Counter Control

Bit No.	7	6	5	4	3	2	1	0
Name	CKSEL1	FRQSEL1	FRQSEL0	ADCLK	DMAEN	TINTE	DINTE	AINTE
Reset	0	0	0	0	0	0	0	0

CKSEL1 Clock source selection for counter/timer 1
FRQSEL1 Input frequency selection for counter/timer 1 when CKSEL1 = 1
FRQSEL0 Input frequency selection for counter/timer 0.
ADCLK A/D trigger select when AINTE = 1
DMAEN Enable DMA operation. 1 = enable, 0 = disable.
TINTE Enable timer interrupts. 1 = enable, 0 = disable.
DINTE Enable digital I/O interrupts. 1 = enable, 0 = disable.
AINTE Enable analog input interrupts. 1 = enable, 0 = disable.

Base + 5 Write FIFO Threshold / FIFO Threshold X8

Bit No.	7	6	5	4	3	2	1	0
Name	X/FT10	X/FT09	FT5/FT08	FT4/FT07	FT3/FT06	FT2/FT05	FT1/FT04	FT0/FT03
Reset	0	0	0	0	0	0	0	0

FT5–0 When EXFIFO = 0 (Basic Mode, See Register Description for Page 2 Base+12)
FT10–03 When EXFIFO = 1 (Enhanced Mode, See Register Description for Page 2 Base+12)

Base + 5 Read FIFO Threshold / FIFO Depth LSB

Bit No.	7	6	5	4	3	2	1	0
Name	X/FD07	X/FD06	FT5/FD05	FT4/FD04	FT3/FD03	FT2/FD02	FT1/FD01	FT0/FD00
Reset	0	0	0	0	0	0	0	0

FT5-0 When EXFIFO = 0 (Basic Mode, See Register Description for Page 2 Base+12)
FD07-00 When EXFIFO = 1 (Enhanced Mode, See Register Description for Page 2 Base+12)

Base + 6 Write DAC LSB

Bit No.	7	6	5	4	3	2	1	0
Name	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
Reset	0	0	0	0	0	0	0	0

DA7–0 — D/A data bits 7 - 0; This register stores the DA LSB. D/A data is an unsigned 12-bit value. This register must be written to before the MSB, since writing the MSB updates the DAC immediately. (Unless DASIM is enabled)

Base + 6 Read A/D Channel and FIFO Status

Bit No.	7	6	5	4	3	2	1	0
Name	FD7/FD11	FD6/FD10	FD5/FD09	FD4/FD08	FD3/OVF	FD2/FF	FD1/HF	FD0/EF
Reset	0	0	0	0	0	0	0	0

FD7–0 When EXFIFO = 0 (Basic Mode, See Register Description for Page 2 Base+12)
FD11–08 When EXFIFO = 1 (Enhanced Mode, See Register Description for Page 2 Base+12)

OVF	FIFO Overflow bit.
FF	FIFO Full Bit. The next conversion will result in an overflow.
HF	FIFO Half Full Bit. FIFO is at least half full containing at least 1k words of A/D data.
EF	FIFO Empty. FIFO is empty.

Base + 7 Write DAC MSB

Bit No.	7	6	5	4	3	2	1	0
Name	DACH1	DACH0	-	-	DA11	DA10	DA9	DA8
Reset	0	0	0	0	0	0	0	0

DACH1–0 D/A channel. The values written to Base + 6 and Base + 7 update the selected channel immediately unless DASIM is enabled. The update takes approximately 50ns due to the DAC serial interface.

DA11–8 D/A bits 11 - 8; DA11 is the MSB. D/A data is an unsigned 12-bit value. Writing to this register updates the DAC (If DASIM is disabled).

Base + 7 Read Analog Operation Status

Bit No.	7	6	5	4	3	2	1	0
Name	-	TINT	DINT	AINT	ADCH3	ADCH2	ADCH1	ADCH0
Reset	0	0	0	0	0	0	0	0

TINT Timer interrupt status, 1 = interrupt pending, 0 = interrupt not pending.

DINT Digital I/O interrupt status, 1 = interrupt pending, 0 = interrupt not pending.

AINT Analog input interrupt status, 1 = interrupt pending, 0 = interrupt not pending.

ADCH3-0 Current A/D channel. This is the channel that will be sampled on the next conversion.

Base + 8 Read/Write Digital I/O Port A

Bit No.	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0
Reset	0	0	0	0	0	0	0	0

These registers are used for digital I/O on PortA. The direction of each register is controlled by the DIO control register at Base+11.

Base + 9 Read/Write Digital I/O Port B

Bit No.	7	6	5	4	3	2	1	0
Name	B7	B6	B5	B4	B3	B2	B1	B0
Reset	0	0	0	0	0	0	0	0

These registers are used for digital I/O on PortB. The direction of each register is controlled by the DIO control register at Base+11.

Base + 10 Read/Write Digital I/O Port C

Bit No.	7	6	5	4	3	2	1	0
Name	C7	C6	C5	C4	C3	C2	C1	C0
Reset	0	0	0	0	0	0	0	0

These registers are used for digital I/O on Port C. The direction of each register is controlled by the DIO control register at Base+11.

Base + 11 Write Digital I/O and DA Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	DIOCTR		DASIM	DIRA	DIRCH	-	DIRB	DIRCL
Reset	1	X	0	1	1	0	1	1

DIOCTR selects the function of 4 bits in DIO port C:

<i>Pin No.</i>	<i>DIOCTR = 0</i>	<i>DIOCTR = 1</i>
21	PC4Gate 0	DIO PC4
22	PC5Gate 1	DIO PC5
23	PC6 Clk 1	DIO PC6
24	PC7 Out 0	DIO PC7

NOTE: If DIOCTR = 1, then the pin direction is controlled by DIRCH.

- DIRA Port A direction. 0 = output, 1 = input
- DIRB Port B direction: 0 = output, 1 = input
- DIRCH Port C bits 7-4 direction: 0 = output, 1 = input
- DIRCL Port C bits 3-0 direction: 0 = output, 1 = input
- DASIM DASIM D/A simultaneous update control. This bit determines when the D/A is updated.

Base + 11 Read Digital I/O and DA Control Register Readback

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	DASIM	DIRA	DIRCH	-	DIRB	DIRCL
Reset	0	0	0	0	0	0	0	0

Read-back of Base+11.

5.1.5. Page 0: Counter / Timer Control Registers
Page 0, Base + 12 Read/Write Counter/Timer D7 - 0

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD7	CTRD6	CTRD5	CTRD4	CTRD3	CTRD2	CTRD1	CTRD0
Reset	0	0	0	0	0	0	0	0

This register is used for both Counter 0 and Counter 1. It is the LSB for both counters.

Page 0, Base + 13 Read/Write Counter/Timer D15 - 8

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD15	CTRD14	CTRD13	CTRD12	CTRD11	CTRD10	CTRD9	CTRD8
Reset	0	0	0	0	0	0	0	0

This register is used for both Counter 0 and Counter 1. It is the MSB for counter 1 and the middle byte for counter 0.

Page 0, Base + 14 Read/Write Counter/Timer D23 - 16

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD23	CTRD22	CTRD21	CTRD20	CTRD19	CTRD18	CTRD17	CTRD16
Reset	0	0	0	0	0	0	0	0

This register is used for Counter 0 only. Counter 0 is 24 bits wide, while Counter 1 is only 16 bits wide.

Page 0, Base + 15 Write Counter/Timer Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	CTRNO	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR
Reset	0	0	0	0	0	0	0	0

- CTRNO Counter no., 0 or 1
- LATCH Latch the selected counter so that its value may be read.
- GTDIS Disable external gating for the selected counter.
- GTEN Enable external gating for the selected counter.
- CTDIS Disable counting on the selected counter. The counter will ignore input pulses.
- CTEN Enable counting on the selected counter. The counter will decrement on each input pulse.
- LOAD Load the selected counter with the data written to Base + 12 through Base + 14 or Base + 12 and Base + 13 (depending on which counter is being loaded).
- CLR Clear the current counter (set its value to 0).

Page 0, Base + 15 Read FPGA Revision Code

Bit No.	7	6	5	4	3	2	1	0
Name	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0
Reset	0	0	0	0	0	0	0	0

REV7-0 — Revision code, read as a 2-digit hex value. The first rev of this FPGA should be 0x48.

5.1.6. Page 1: Autocalibration Control Registers

Page 1, Base + 12 Read/Write EEPROM / TrimDAC Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
Reset	0	0	0	0	0	0	0	0

D7-0 — Calibration data to be read or written to the EEPROM and/or TrimDAC.

Page 1, Base + 13 Read/Write EEPROM / TrimDAC Address Register

Bit No.	7	6	5	4	3	2	1	0
Name	X	A6	A5	A4	A3	A2	A1	A0
Reset	0	0	0	0	0	0	0	0

A6-A0 — EEPROM / TrimDAC address.

Page 1, Base + 14 Write Calibration Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	EE_EN	EE_RW	RUNCAL	CALMUX	TDACEN	X	X	X
Reset	0	0	0	0	0	0	0	0

EE_EN EEPROM Enable. Writing a 1 to this bit will initiate a transfer to/from the EEPROM as indicated by the EE_RW bit.

EE_RW Selects read or write operation for the EEPROM: 0 = Write, 1 = Read.

RUNCAL Writing 1 to this bit causes the board to reload the calibration settings from EEPROM.

CALMUX Calibration multiplexor enable.

TDACEN TrimDAC Enable. Writing 1 to this bit will initiate a transfer to the TrimDAC (used in the autocalibration process).

Page 1, Base + 14 Read Calibration Status Register

Bit No.	7	6	5	4	3	2	1	0
Name	0	TDBUSY	EEBUSY	CALMUX	TDACEN	0	0	0
Reset	0	0	0	0	0	0	0	0

TDBUSY TrimDAC busy indicator

EEBUSY EEPROM busy indicator

Page 1, Base + 15 Write EEPROM Access Key Register

Value	Function
0xA5	The user must write the value 0xA5 (binary 10100101) to this register each time after setting the PAGE bit in order to get access to the EEPROM.
0xA6	Writing 0xA6 to this register unlocks (enables) all enhanced features and sets FIFO depth to 1024 samples.
0xA7	Writing 0xA7 to this register locks (disables) all enhanced features.

Page 1, Base + 15 Read Page 1 ID Read-back

Register	Read-back
Page 1 ID	0xA1

5.1.7. Page 2: Expanded FIFO and AD/DA Control
Page 2, Base + 12 Read/Write Expanded FIFO Control

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	EXFIFO
Reset	0	0	0	0	0	0	0	0

EXFIFO Expanded FIFO enable. Default and reset value is 0, it is also set to 0 when enhanced features are disabled.

When EXFIFO is enabled (EXFIFO=1) dynamic threshold and depth tracking are disabled. The FIFO can then be tracked with the registers at base+6.

Page 2, Base + 13 Read/Write AD/DA Mode Control

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	DACPOLE N	DACPOL	ADPOL	ADPOLEN	ADSD	ADSDEN
Reset	0	0	0	0	0	0	0	0

ADPOL Unipolar output setting. Set this bit (ADPOL=1) for Unipolar operation, clear this bit for Bipolar operation.

ADPOLEN Enable ADPOL. When this bit is set, the ADPOL setting is output to the DAQ circuit.

ADSD Single Ended / Differential output setting. Set this bit (ADSD=1) for Single Ended operation, clear this bit for Differential operation.

ADSDEN Enable ADSD. When this bit is set, the ADSD setting is output to the DAQ circuit.

DACPOLEN Enable DACPOL. When this bit is set, the DACPOL setting is output to the DAC circuit.

DACPOL DAC Polarity software override.

DACPOLEN

Value	Description
0	DAC Polarity is controlled by jumpers (Default power on setting – DACLSEL pin in tri-state mode)
1	DAC Polarity is controlled by software using DACPOL bit setting.

DACPOL

Value	Description
0	DAC is set in UNIPOLAR mode
1	DAC is set in BIPOLAR mode

Page 2, Base + 14 Read/Write AD Scan Interval

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	SCANINT
Reset	0	0	0	0	0	0	0	0

SCANINT	Description
0	10us (default)
1	5us

On power-up or reset, SCANINT returns to its default value of 0.

Page 2, Base + 15 Write DAQ LED Control

Bit No.	7	6	5	4	3	2	1	0
Name	DAQ_LED	-	-	SERCFG	SC3	SC2	SC1	SC0
Reset	0	0	0	0	EEPROM	EEPROM	EEPROM	EEPROM

DAQ_LED This signal controls the Blue LED (FPGA_LED) on the board. It should be set to 0 once the DAQ is configured and ready for use by the user.

SERCFG Serial port configuration control; on power-up / reset these bits are loaded from the EEPROM

SC3-0 Serial port protocol configuration bits; these control the values on I/O pins P_SC3-0

DAQ_LED

Value	Description
0	LED ON (Default)
1	LED OFF

SERCFG

Value	Description
1	ignore DAQ_LED bit and write SC3-0 bits to serial configuration register
0	write DAQ_LED bit and ignore SC3-0 bits

Ports 1-2

	SC1	SC0
Internal loop back	0	0
RS485	0	1
RS232	1	0
RS422	1	1

Ports 3-4

	SC3	SC2
Internal loop back	0	0
RS485	0	1
RS232	1	0
RS422	1	1

Page 2, Base + 15 Read

Register	Read-back
Page 2 ID	0xA2

Page 2 ID Read-back

This register may be read back to confirm accesses to page 2. The register returns 0xA2.

5.1.8. Page 3: Board IDs

Page 3, Base + 12 Write

This is a Read only register

Any writes to this register are discarded.

Page 3, Base + 12 Read

RESERVED

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-
Reset	0	0	0	0	0	0	0	0

This register provides a readback of 0x00 after RESET.

Page 3, Base + 13 Write

This is a Read only register

Any writes to this register are discarded.

Page 3, Base + 13 Read RESERVED

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-
Reset	0	0	0	0	0	0	0	0

This register provides a readback of 0x00 after RESET.

Page 3, Base + 14 Write This is a Read only register

Any writes to this register are discarded.

Page 3, Base + 14 Read Board Minor ID

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-
Reset	0	0	0	0	0	0	0	1

This register may be read back to confirm accesses to page 3, FPGA Minor ID is 0x01.

Page 3, Base + 15 Write This is a Read only register

Any writes to this register are discarded.

Page 3, Base + 15 Read Board Major ID

Bit No.	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	-	-
Reset	0	0	0	1	0	1	1	0

6. A/D Circuit

6.1. Analog-to-Digital Input Ranges and Resolution

6.1.1. Overview

Athena IV uses a 16-bit A/D converter. The full range of numerical values for a 16-bit number is 0 - 65535. However, the A/D converter uses two's complement notation, so the A/D value is interpreted as a signed integer, ranging from -32768 to +32767.

The smallest change in input voltage that can be detected is $1/(2^{16})$, or $1/65536$, of the full-scale input range. This smallest change results in an increase or decrease of 1 in the A/D code, and is referred to as 1 LSB (1 Least Significant Bit).

The analog inputs on Athena IV have three configuration options.

- Single-ended or differential mode
- Unipolar or bipolar mode
- Input range (gain)

The single-ended/differential and unipolar/bipolar modes are configured using jumper block J13, and apply to all inputs. The input range selection is done in software.

6.1.1.1. Input Range Selection

You can select a gain setting for the inputs, which causes them to be amplified before they reach the A/D converter. The gain setting is controlled in software, which allows it to be changed on a channel-by-channel basis. In general, you should select the highest gain (smallest input range) that allows the A/D converter to read the full range of voltages over which the input signals will vary. However, a gain that is too high causes the A/D converter to clip at either the high end or low end, and you will not be able to read the full range of voltages on your input signals.

6.1.1.2. Input Range Table

The table below indicates the analog input range for each possible configuration. The polarity is set using jumper block J13, and the gain is set with the G1 and G0 bits in the register at Base+3. The Gain value in the table is provided for clarity. Note that the single-ended vs. differential setting has no impact on the input range or the resolution.

<i>Polarity</i>	<i>G1</i>	<i>G0</i>	<i>Input Range</i>	<i>Resolution 1LSB</i>
Bipolar	0	0	±10V	305µV
Bipolar	0	1	±5V	153µV
Bipolar	1	0	±2.5V	76µV
Bipolar	1	1	±1.25V	38µV
Unipolar	0	0	Invalid	Invalid
Unipolar	0	1	0 - 10V	153µV
Unipolar	1	0	0 - 5V	76µV
Unipolar	1	1	0 - 2.5V	38µV

6.2. Performing an A/D Conversion

6.2.1. Introduction

This chapter describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (without the driver software). Perform an A/D conversion according to the following steps. Each step is discussed in detail, below.

- Select the input channel.
- Select the input range.
- Wait for analog input circuit to settle.
- Initiate an A/D conversion.
- Wait for the conversion to finish.
- Read the data from the board.
- Convert the numerical data to a meaningful value.

6.2.2. Select the Input Channel

To select the input channel to read, write a low-channel/high-channel pair to the channel register at Base+2. The low four bits select the low channel, and the high four bits select the high channel. When you write any value to this register, the current A/D channel is set to the low channel.

For example, to set the board to channel 4 only, write 0x44 to Base+2). To set the board to read channels 0 through 15, write 0xF0 to Base+2.

When you perform an A/D conversion, the current channel automatically increments to the next channel in the selected range. Therefore, to perform A/D conversions on a group of consecutively-numbered channels, you do not need to write the input channel prior to each conversion. For example, to read from channels 0 - 2, write 0x20 to base+2. The first conversion is on channel 0, the second will be on channel 1 and the third will be on channel 2. The channel counter wraps around to the beginning so the fourth conversion will be on channel 0, again.

If you are sampling the same channel repeatedly, set both high and low to the same value as in the first example, above. On subsequent conversions, you do not need to set the channel again.

6.2.3. Select the Input Range

Select the input range from among the available ranges. If the range is the same as for the previous A/D conversion it does not need to be set again. Write this value to the input range register at Base+3.

For example, for $\pm 5V$ range (gain of 2), write 0x01 to Base+3.

6.2.4. Wait for Analog Input Circuit to Settle

After writing to the channel register, Base+2, or the input range register, Base+3, allow time for the analog input circuit to settle before starting an A/D conversion. The board has a built-in 10 μ S timer to assist with the wait period. Monitor the WAIT bit at Base+3, bit 5. When the bit value is 1, the circuit is actively settling on the input signal. When the value is 0, the board is ready to perform A/D conversions.

6.2.5. Perform an A/D Conversion on the Current Channel

After the above steps are completed, start the A/D conversion by writing to Base+0. This write operation only triggers the A/D if AINTE = 0 (interrupts are disabled). When AINTE = 1, the A/D can only be triggered by the on-board counter/timer or an external signal. This protects against accidental triggering by software during a long-running interrupt-based acquisition process.

```
outp(base,0x80);
```

6.2.6. Wait for the Conversion to Finish

The A/D converter chip takes up to five microseconds to complete one A/D conversion. Most processors and software can operate fast enough so that if you try to read the A/D converter immediately after starting the conversion, the read will occur faster than the A/D conversion and return invalid data. Therefore, the A/D converter provides a status signal to indicate whether it is busy or idle. This bit can be read back from the status register at Base+3, bit 7. When the A/D converter is busy (performing an A/D conversion), the bit value is 1 and the program must wait. When the A/D converter is idle (conversion is done and data is available), this bit value is 0 and the program may read the data.

The following statement is a simple example of this operation.

```
while (inp(base+3) & 0x80); // Wait for conversion to finish before proceeding
```

The above example could hang your program if there is a hardware fault and the bit is stuck at 1. A better solution is to use a loop with a timeout, as shown below.

```
int checkstatus() // returns 0 if ok, -1 if error  
int i;  
for (i = 0; i < 10000; i++)  
{  
    if !(inp(base+3) & 0x80) then return(0);    // conversion completed  
}  
return(-1);                                // conversion did not complete
```

6.2.7. Read the Data from the Board

Once the conversion is complete, you can read the data back from the A/D converter. The data is a 16-bit value and is read back in two 8-bit bytes. The LSB must be read from the board before the MSB because the data is inserted into the board's FIFO in that order. Unlike other registers on the board, the A/D data may only be read one time, because each time a byte is read from the FIFO the internal FIFO pointer advances and that byte is no longer available. Reading data from an empty FIFO returns unpredictable results.

The following pseudo-code illustrates how to read and construct the 16-bit A/D value.

```
LSB = inp(base);  
MSB = inp(base+1);  
Data = MSB * 256 + LSB; // combine the 2 bytes into a 16-bit value
```

The final data are interpreted as a 16-bit signed integer in the range -32768 to +32767.

Note: The data range always includes both positive and negative values, even if the board is set to a unipolar input range. The data must now be converted to volts or other engineering units by using a conversion formula, as discussed below.

In scan mode, the behavior is the same except when the program initiates a conversion, all channels in the programmed channel range will be sampled once and the data will be stored in the FIFO. The FIFO depth register increments by the scan size. When STS goes low, the program should read out the data for all channels.

6.2.8. Convert the numerical data to a meaningful value

Once the A/D value is read, it needs to be converted to a meaningful value. The first step is to convert it back to the actual measured voltage. Afterwards, you may need to convert the voltage to some other engineering units. For example, the voltage may come from a temperature sensor and the voltage would then need to be converted to the corresponding temperature, according to the temperature sensor's characteristics.

Since there are a large number of possible input devices, this secondary step is not included here. Only conversion to input voltage is described. However, you can combine both transformations into a single formula if desired.

To convert the A/D value to the corresponding input voltage, use the following formulas.

6.2.8.1. Conversion Formula for Bipolar Input Ranges

$$\text{Input voltage} = \text{A/D value} / 32768 * \text{Full-scale input range}$$

Example:

Given, Input range is $\pm 5\text{V}$ and A/D value is 17761.

Therefore,

$$\text{Input voltage} = 17761 / 32768 * 5\text{V} = 2.710\text{V}.$$

For a bipolar input range,

$$1 \text{ LSB} = 1/32768 * \text{Full-scale voltage}.$$

The table, below, shows the relationship between A/D code and input voltage for a bipolar input range (V_{FS} = Full scale input voltage).

<i>A/D Code</i>	<i>Input Voltage Symbolic Formula</i>	<i>Input Voltage for $\pm 5\text{V}$ Range</i>
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS} + 1 \text{ LSB}$	-4.9998V
...	...	...
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
...	...	...
32767	$V_{FS} - 1 \text{ LSB}$	4.9998V

6.2.8.2. Conversion Formula for Unipolar Input Ranges

$$\text{Input voltage} = (\text{A/D value} + 32768) / 65536 * \text{Full-scale input range}$$

Example:

Given, Input range is 0-5V and A/D value is 17761.

Therefore,

$$\text{Input voltage} = (17761 + 32768) / 65536 * 5\text{V} = 3.855\text{V}.$$

For a unipolar input range, $1 \text{ LSB} = 1/65536 * \text{Full-scale voltage}$.

The following table illustrates the relationship between A/D code and input voltage for a unipolar input range (VFS = Full scale input voltage).

A/D Code	Input Voltage Symbolic Formula	Input Voltage for 0–5V Range
-32768	0V	0.0000V
-32767	1 LSB ($V_{FS} / 65536$)	0.000076V
...	...	...
-1	$V_{FS} / 2 - 1 \text{ LSB}$	2.4999V
0	$V_{FS} / 2$	2.5000V
1	$V_{FS} / 2 + 1 \text{ LSB}$	2.5001V
...	...	...
32767	$V_{FS} - 1 \text{ LSB}$	4.9999V

6.3. A/D Scan, Interrupt and FIFO Operation

The control bits SCANEN (scan enable) and AINTE (A/D interrupt enable) in conjunction with the FIFO determine the behavior of the board during A/D conversions and interrupts.

At the end of an AD conversion, the 16-bit A/D data is latched into the 8-bit FIFO in an interleaved fashion: first LSB, then MSB. A/D Data is read out of the FIFO with 2 read operations, first Base + 0 (LSB) and then Base + 1 (MSB).

When SCANEN = 1, each time an A/D trigger occurs, the board will perform an A/D conversion on all channels in the channel range programmed in Base + 2. When SCANEN = 0, each time an A/D trigger occurs, the board will perform a single A/D conversion and then advance to the next channel and wait for the next trigger.

During interrupt operation (AINTE = 1), the FIFO will fill up with data until it reaches the threshold programmed in the FIFO threshold register, and then the interrupt request will occur. If AINTE = 0, the FIFO threshold is ignored and the FIFO continues to fill up.

If the FIFO reaches its limit of 48 samples, then the next time an A/D conversion occurs the Overflow flag OVF will be set. In this case the FIFO will not accept any more data, and its contents will be preserved and may be read out. In order to clear the overflow condition, the program must reset the FIFO by writing to the FIFORST bit in Base + 1, or a hardware reset must occur.

In Scan mode (SCANEN = 1), the FIFO threshold should be set to a number at least equal to the scan size and in all cases equal to an integral number of scans. For example if the scan size is 8 channels, the FIFO threshold should be set to 8, 16, 24, 32, 40, or 48, but not less than 8. This way the interrupt will occur at the end of the scan, and the interrupt routine can read in a complete scan or set of scans each time it runs.

In non-scan mode (SCANEN = 0), the FIFO threshold should be set to a level that minimizes the interrupt rate but leaves enough time for the interrupt routine to respond before the next A/D conversion occurs. Remember that no data is available until the interrupt occurs, so if the rate is slow the delay to receive A/D data may be long. Therefore for slow sample rates the FIFO threshold should be small. If the sample rate is high, the FIFO threshold should be high to reduce the interrupt rate. However remember that the remaining space in the FIFO determines the time the interrupt routine has to respond to the interrupt request. If the FIFO threshold is too high, the FIFO may overflow before the interrupt routine responds. A good rule of thumb is to limit the interrupt rate to no more than 1,000-2,000 per second in Windows and Linux or 10,000 per second in DOS. Experimentation may be necessary to determine the optimum FIFO threshold for each application.

The table on the next page describes the board's behavior for each of the 4 possible cases of AINTE and SCANEN. The given interrupt software behavior describes the operation of the Diamond Systems Universal Driver software. If you write your own software or interrupt routine you should conform to the described behavior for optimum results.

The following table describes the register settings for the A/D operating modes. (LOW and HIGH channels referenced in the table are the 4-bit channel numbers in Base+2.)

<i>AINTE</i> <i>Base+4,</i> <i>bit 0</i>	<i>SCANE</i> <i>Base+2,</i> <i>bit 1</i>	<i>Operation</i>
0	0	Single A/D conversions are triggered by write to B+0. STS stays high during the A/D conversion. No interrupt occurs. The user program monitors STS (Base+3, bit 7) and reads A/D data when STS goes low.
0	1	A/D scans are triggered by write to B+0. All channels between LOW and HIGH are sampled. STS stays high during the entire scan (multiple A/D conversions). No interrupt occurs. The user program monitors STS (Base+3, bit 7) and reads A/D data when STS goes low.
1	0	Single A/D conversions are triggered by the source selected with ADCLK (Base+4, bit 4). STS stays high during the A/D conversion. A/D interrupt occurs when the FIFO reaches its programmed threshold. The interrupt routine reads the number of samples equal to the FIFO threshold (Base+5, bits 0-5).
1	1	A/D scans are triggered by the source selected with ADCLK (Base+4, bit 4). STS stays high during the entire scan (multiple A/D conversions). A/D interrupt occurs when the FIFO reaches its programmed threshold. The interrupt routine reads the number of samples equal to the FIFO threshold (Base+5, bits 0-5).

7. D/A Circuit

7.1. Digital-to-Analog Output Ranges and Resolution

7.1.1. Description

uses a 4-channel 12-bit D/A converter (DAC) to provide four analog outputs. A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is $2^{12} - 1$, or 4095, so the full range of numerical values that the DACs support is 0 - 4095. The value 0 always corresponds to the lowest voltage in the output range, and the value 4095 always corresponds to the highest voltage minus 1 LSB. The theoretical top end of the range corresponds to an output code of 4096 which is impossible to achieve.

Note: In this manual, the terms analog output, D/A, and DAC are all used interchangeably to mean the conversion of digital data originating from the computer hardware to an analog signal terminating at an external source.

7.1.2. Resolution

The resolution is the smallest possible change in output voltage. For a 12-bit DAC the resolution is $1/(2^{12})$, or $1/4096$, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code, so this change is referred to as 1 least significant bit (1 LSB). The value of this LSB is calculated as follows.

$$1 \text{ LSB} = \text{Output voltage range} / 4096$$

Example:

For, Output range = 0-10V,

$$\text{Output voltage range} = 10\text{V} - 0\text{V} = 10\text{V}$$

Therefore,

$$1 \text{ LSB} = 10\text{V} / 4096 = 2.44\text{mV}$$

Example:

For, Output range = $\pm 10\text{V}$;

$$\text{Output voltage range} = 10\text{V} - (-10\text{V}) = 20\text{V}$$

Therefore,

$$1 \text{ LSB} = 20\text{V} / 4096 = 4.88\text{mV}$$

7.1.3. Output Range Selection

Jumper block J13 is used to select the DAC output range. The DACs can be configured for 0-10V or $10\text{V}_{\pm}$.

Two parameters are configured:

- unipolar/bipolar mode
- power-up/reset clear mode.

In most cases, for unipolar mode configure the board to reset to zero scale, and for bipolar mode configure the board for reset to mid-scale. In each case, the DACs reset to 0V.

7.1.4. D/A Conversion Formulas and Tables

The formulas below explain how to convert between D/A codes and output voltages.

7.1.4.1. D/A Conversion Formulas for Unipolar Output Ranges

$$\text{Output voltage} = (\text{D/A code} / 4096) * \text{Reference voltage}$$

$$\text{D/A code} = (\text{Output voltage} / \text{Reference voltage}) * 4096$$

Example:

For,

Output range in unipolar mode = 0 – 10V,

and,

Full-scale range = 10V – 0V = 10V,

if,

Desired output voltage = 2.000V,

D/A code = $2.000\text{V} / 10\text{V} * 4096 = 819.2 \Rightarrow 819$

Note: the output code is always an integer.

For the unipolar output range 0-10V, 1 LSB = $1/4096 * 10\text{V} = 2.44\text{mV}$.

The following table illustrates the relationship between D/A code and output voltage for a unipolar output range (V_{REF} = Reference voltage).

D/A Code	Output Voltage Symbolic Formula	Output Voltage for 0-10V Range
0	0V	0.0000V
1	1 LSB (V _{REF} / 4096)	0.0024V
...	...	...
2047	V _{REF} / 2 - 1 LSB	4.9976V
2048	V _{REF} / 2	5.0000V
2049	V _{REF} / 2 + 1 LSB	5.0024V
...	...	...
4095	V _{REF} - 1 LSB	9.9976V

7.1.4.2. D/A Conversion Formulas for Bipolar Output Ranges

$$\text{Output voltage} = ((\text{D/A code} - 2048) / 2048) * \text{Output reference}$$

$$\text{D/A code} = (\text{Output voltage} / \text{Output reference}) * 2048 + 2048$$

Example:

For,

Output range in bipolar mode = $\pm 10\text{V}$

and,

Full-scale range = 10V – (-10V) = 20V

if,

Desired output voltage = 2.000V

D/A code = $2\text{V} / 10\text{V} * 2048 + 2048 = 2457.6 \Rightarrow 2458$

For the bipolar output range $\pm 10\text{V}$, 1 LSB = $1/4096 * 20\text{V}$, or 4.88mV.

The following table illustrates the relationship between D/A code and output voltage for a bipolar output range (V_{REF} = Reference voltage).

<i>D/A Code</i>	<i>Output Voltage Symbolic Formula</i>	<i>Output Voltage for $\pm 10V$ Range</i>
0	$-V_{REF}$	-10.0000V
1	$V_{REF} + 1 \text{ LSB}$	-9.9951V
...	...	...
2047	-1 LSB	-0.0049V
2048	0	0.0000V
2049	+1 LSB	0.0049V
...	...	...
4095	$V_{REF} - 1 \text{ LSB}$	9.9951V

7.2. Generating an Analog Output

There are three steps involved in performing a D/A conversion, or generating an analog output. Each step is described in more detail, below. The descriptions use direct programming instead of driver software.

Compute the D/A code for the desired output voltage.

- Write the value to the selected output channel.
- Wait for the D/A to update.

7.2.1. Compute the D/A Code for the Desired Output Voltage

Use the formulas in the preceding section to compute the D/A code required to generate the desired voltage.

Note: The DAC cannot generate the actual full-scale reference voltage; to do so would require an output code of 4096, which is not possible with a 12-bit number. The maximum output value is 4095. Therefore, the maximum possible output voltage is always 1 LSB less than the full-scale reference voltage.

7.2.2. Write the Value to the Selected Output Channel Registers

Use the following formulas to compute the LSB and MSB values.

LSB = D/A Code & 255 ;keep only the low 8 bits

MSB = int(D/A code / 256) ;strip off low 8 bits, keep 4 high bits

Example:

For,

Output code = 1776

Compute,

LSB = 1776 & 255 = 240 (0xF0)

and

MSB = int(1776 / 256) = int(6.9375) = 6

The LSB is an 8-bit number in the range 0-255. The MSB is a 4-bit number in the range 0-15.

The MSB is always rounded down. The truncated portion is accounted for by the LSB.

Write these values to the selected channel. The LSB is written to Base+6. The MSB and channel number are written to Base+7 (MSB = bits 0-3, channel number, 0-3 = bits 6-7).

```
outp(Base+6, LSB);  
outp(Base+7, MSB + channel << 6);
```

7.2.3. Wait for the D/A to Update

Writing the MSB and channel number to Base+7 starts the D/A update process for the selected channel. The update process requires approximately 30 microseconds to transmit the data serially to the D/A chip and update the D/A circuit in the chip. During this period, no attempt should be made to write to any other channel in the D/A through addresses Base+6 or Base+7.

The status bit DACBUSY (Base+3, bit 4) indicates if the D/A is busy updating (1) or idle (0). After writing to the D/A, monitor DACBUSY until it is zero before continuing with the next D/A operation.

7.3. Analog Circuit Calibration

The Athena IV data acquisition circuit contains an advanced autocalibration circuit that can maintain the accuracy of both A/D and D/A circuits to within the specified tolerances regardless of time and temperature. Autocalibration is supported in the Diamond Systems Universal Driver software included with the board.

The autocalibration circuit uses an ultra-stable +5V reference voltage IC as the source for its calibration. Both A/D and D/A circuits are calibrated in the analog domain by using a series of 8-bit “TrimDACs” to adjust the offset and gain settings of the circuits. The data values driving the DACs are stored in an EEPROM and are loaded automatically each time the board powers up.

During the autocalibration process, the board will measure the on-board reference and calibrate the A/D circuit by adjusting the TrimDACs to achieve the best accuracy. Once the A/D circuit is calibrated, the D/A circuit is calibrated by routing the D/A outputs into the A/D converter and adjusting them as well. The new calibration values for the TrimDACs are stored back into the EEPROM so they can be automatically recalled thereafter.

A unique feature of Diamond’s autocalibration process is that each analog input range is individually calibrated for optimum performance. Analog amplifier circuits with 16-bit accuracy exhibit gain and offset errors that vary depending on the gain setting. The settings that work best for one range may not be sufficient to calibrate another. If a circuit is calibrated for maximum accuracy in a particular input range, such as +/-5V, changing the input range to +/-10V or 0-2.5V may introduce errors that exceed the resolution of a 16-bit measurement and will require calibration again.

To counteract this phenomenon, Diamond’s autocalibration circuit provides for a separate complete set of calibration settings for each analog input range. During the autocalibration process, each range is calibrated one at a time, and its set of calibration settings is stored in a separate area of the EEPROM’s memory. One of these ranges is identified as the “boot range”, and this range’s calibration values are the ones that are automatically recalled during power-up. You have the option of specifying the boot range, which should be chosen as the range most commonly used in your application. When you change the input range, you have the option of loading the calibration values for the new input range to maintain optimum accuracy of your measurements.

The autocalibration process is triggered with a single function call in the Diamond Universal Driver software. The process takes about 10-20 seconds to calibrate the complete set of analog input ranges and about the same time for the D/A circuit. Autocalibration can easily be incorporated into your application program, so that you can calibrate the data acquisition circuit as often as necessary while your system is running.

8. Digital I/O

8.1. Digital I/O Operation

Athena IV contains 24 digital I/O lines organized as three 8-bit I/O ports: Port A, Port B, and Port C. The direction of each port is programmable, and port C is further divided into two 4-bit halves, each with independent direction. The port data are accessed at registers Base+8 through Base+10, and the port direction register is located at Base+11.

Base +	7	6	5	4	3	2	1	0
8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
9	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
10	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
11	DIOCTR	-	-	DIRA	DIRCH	-	DIRB	DIRCL

The digital I/O lines are located at pins 1 through 24 on the I/O header J14. The lines are 3.3V and 5V logic compatible. Each output is capable of supplying –8mA in logic 1 state and +12mA in logic 0 state.

DIRA, DIRB, DIRCH, and DIRCL control the direction of ports A, B, C4-7 and C0-3. A direction value of 0 means output and 1 means input. All ports power up to input mode and the output registers are cleared to zero. When a port direction is changed to output, its output register is cleared to zero. When a port is in output mode, its value can be read back.

DIOCTR is used to control the function of lines C7-C4 on the I/O connector. When DIOCTR = 1, the lines are port C7-C4. When DIOCTR = 0, the lines are used for the counter/timer.

Pin No.	DIOCTR = 1	DIOCTR = 0	Pin direction for DIOCTR = 0
21	C4	Gate0	Input
22	C5	Gate1	Input
23	C6	Clk1	Input
24	C7	Out0	Output

9. Counters and Timers

9.1. Counter/Timer Operation

Athena IV contains two counter/timers that provide various timing functions on the board for A/D timing and user functions. These counters are controlled with registers in the on-board data acquisition controller FPGA.

9.1.1. Counter 0 – A/D Sample Control

Counter 0 is a 24-bit, “divide-by-n” counter used for controlling A/D sampling. The counter has a clock input, a gate input, and an output. The input is a 10MHz or 1MHz clock provided on the board and selected with bit CKFRQ0 in register Base+4, bit 5. The gate is an optional signal that can be input on pin 21 of I/O header J23 when DIOCTR (Base+11, bit 7) is 0. If this signal is not used, the counter runs freely. The output is a positive pulse whose frequency is equal to the input clock divided by the 24-bit divisor programmed into the counter. The output appears on pin 24 of the I/O header when DIOCTR is 0.

The counter operates by counting down from the programmed divisor value. When the counter reaches zero, it outputs a positive-going pulse equal to one input clock period (100ns or 1μs, depending on the input clock selected by CKFRQ0). The counter then reloads to the initial load value and repeats the process, indefinitely.

The output frequency can range from 5MHz (10MHz clock, divisor = 2) to 0.06Hz (1MHz clock divided by 16,777,215, or 224-1). The output is fed into the A/D timing circuit and can be selected to trigger A/D conversions when Base+4 register bits AINTE is 1 and ADCLK is 0. Using the control register at Base+15, the counter can be loaded, cleared, enabled and disabled. The optional gate can be enabled and disabled and the counter value can be latched for reading.

9.1.2. Counter 1 – Counting/Totalizing Functions

Counter 1 is similar to Counter 0 except that it is a 16-bit counter. Counter 1 also has an input, a gate and an output. These signals may be user-provided on the I/O header when DIOCTR is 0, or the input may come from the on-board clock generator. When the on-board clock generator is used, the clock frequency is either 10MHz or 100KHz, as determined by control Base+4 register bit CKFRQ1.

The output is a positive-going pulse that appears on pin 26 of the I/O header. The output pulse occurs when the counter reaches zero. When the counter reaches zero, it reloads and restarts on the next clock pulse. The output stays high for the entire time the counter is at zero; i.e., from the input pulse that causes the counter to reach zero until the input pulse that causes the counter to reload.

When DIOCTR is 0, Counter 1 operates as follows.

- It counts positive edges of the signal on pin 23 on the I/O header.
- The gate is provided on pin 22. If the signal is high, the counter counts. If the signal is low, the counter holds its value and ignores input pulses. This pin has a pull-up so the counter can operate without any external gate signal.

NOTE: When counting external pulses, Counter 1 only updates its read register every fourth pulse. This behavior is due to the synchronous design of the counter having to contend with the asynchronous input pulses. The count register contents are correct on the fourth pulse but remain static until four additional pulses occur on the input.

When DIOCTR is 1, Counter 1 operates as follows.

The counter takes its input from the on-board clock generator based on the value of the Base+4 register CKFRQ1 bit. There is no gating and the counter runs continuously.

Counter 1 may be used as either a pulse generator or a totalizer/counter. In pulse generator mode, the output signal on pin 26 is of interest. In totalizer/counter mode, the counter value is of interest and may be read by first latching the value and then reading it. The width of the pulse is equal to the time period of the selected counters clock source.

9.1.3. Command Sequences

Diamond Systems provides driver software to control the counter/timers on . The information in this section is intended as a guide for programmers writing their own code, instead of using the driver, and to give a better understanding of the counter/timer operation.

The counter control register is located at I/O address base+15.

9.1.3.1. Load and Enable (Run) a Counter Sequence

- Write the data to the counter. For counter 0, three bytes are required to load a 24-bit value. For counter 1, two bytes are needed for a 16-bit value. The value is an unsigned integer.

Break the load value into 3 bytes: low, middle, and high, (Two bytes for Counter 1) and write the bytes to the data registers in any sequence.

Counter 0:	Counter 1:
outp(base+12,low);	outp(base+12,low);
outp(base+13,middle);	outp(base+13,high);
outp(base+14,high);	

- Load the counter.

Counter 0:	Counter 1:
outp(base+15,0x02);	outp(base+15,0x82);

- Enable the gate if desired. The gating may be enabled or disabled at any time. When gating is disabled, the counter counts all incoming edges. When gating is enabled, if the gate is high the counter counts all incoming edges and, if the gate is low, the counter ignores incoming clock edges.

Counter 0:	Counter 1:
outp(base+15,0x10);	outp(base+15,0x90);

- Enable the counter. A counter may be enabled or disabled at any time. If disabled, the counter ignores incoming clock edges.

Counter 0:	Counter 1:
outp(base+15,0x04);	outp(base+15,0x84);

9.1.3.2. Read a Counter Sequence

- Latch the counter.

Counter 0:	Counter 1:
outp(base+15,0x40);	outp(base+15,0xC0);

- Read the data.

The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1).

Counter 0:	Counter 1:
low=inp(base+12);	low=inp(base+12);
middle=inp(base+13);	high=inp(base+13);
high=inp(base+14);	

- Assemble the bytes into the complete counter value.

Counter 0:	Counter 1:
------------	------------

val = high * 216 + middle * 28 + low; val = high * 28 + low;

9.1.3.3. Disabling the Counter Gate Command

- Disabling the counter gate, as shown below, causes the counter to run continuously.

Counter 0:

outp(base+15,0x20);

Counter 1:

outp(base+15,0xA0);

9.1.3.4. Clearing a Counter Sequence

Clear a counter to restart an operation. Normally, a counter is only cleared after stopping (disabling) and reading the counter. If you clear a counter while it is enabled, it continues to count incoming pulses so the counter value may not remain at zero.

- Stop (disable) the counter.

Counter 0:

outp(base+15,0x08);

Counter 1:

outp(base+15,0x88);

- Read the data (optional).

The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1).

Counter 0:

low=inp(base+12);

Counter 1:

low=inp(base+12);

middle=inp(base+13);high=inp(base+13);

high=inp(base+14);

- Clear the counter.

Counter 0:

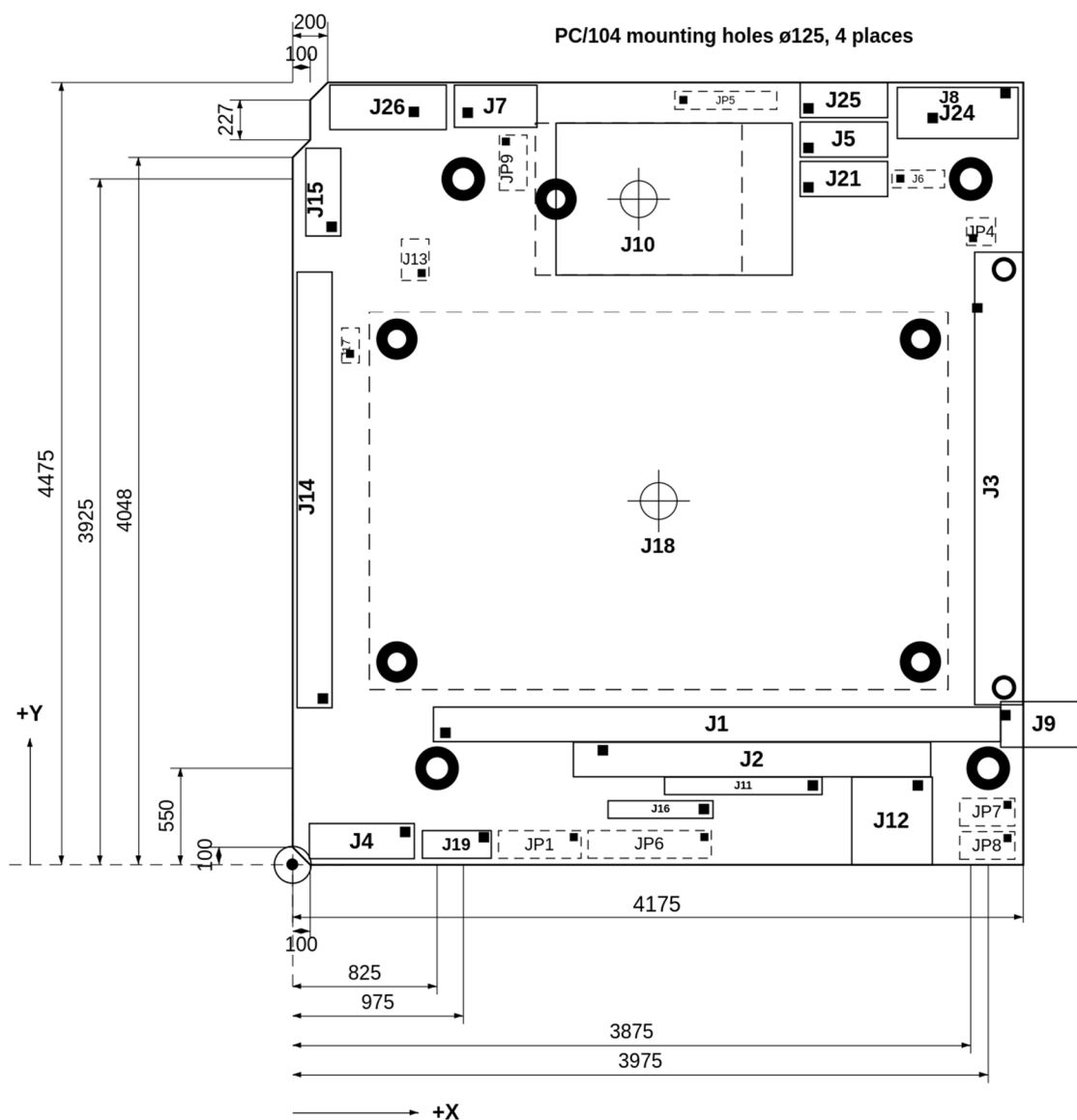
outp(base+15,0x01);

Counter 1:

outp(base+15,0x81);

10. Mechanical Drawing

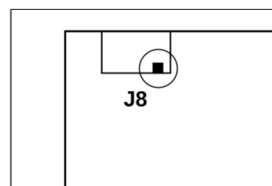
The illustration below provides the dimensions of the key connectors and features of Athena IV.



DATUM X 0, Y 0

Theoretical corner formed by the bottom and left board edges. All coordinates are in mils, measured from this point.

DETAIL — BOTTOM SIDE



Viewed from the bottom of the board, not through it.
X is mirrored relative to the main view.

J8 LCD backlight is the only component on the underside
Pin 1 at X 3660, Y 4270 in board coordinates.

Body outline is nominal, taken from the silkscreen.

11. Connector and Jumper Locations

The Athena IV PCB design includes locations to mount 0 ohm resistors in place of all jumpers to provide a more rugged shock- and vibration-resistant assembly. Contact the Diamond Systems Sales department for information on ordering this option.

11.1. Jumper Locations

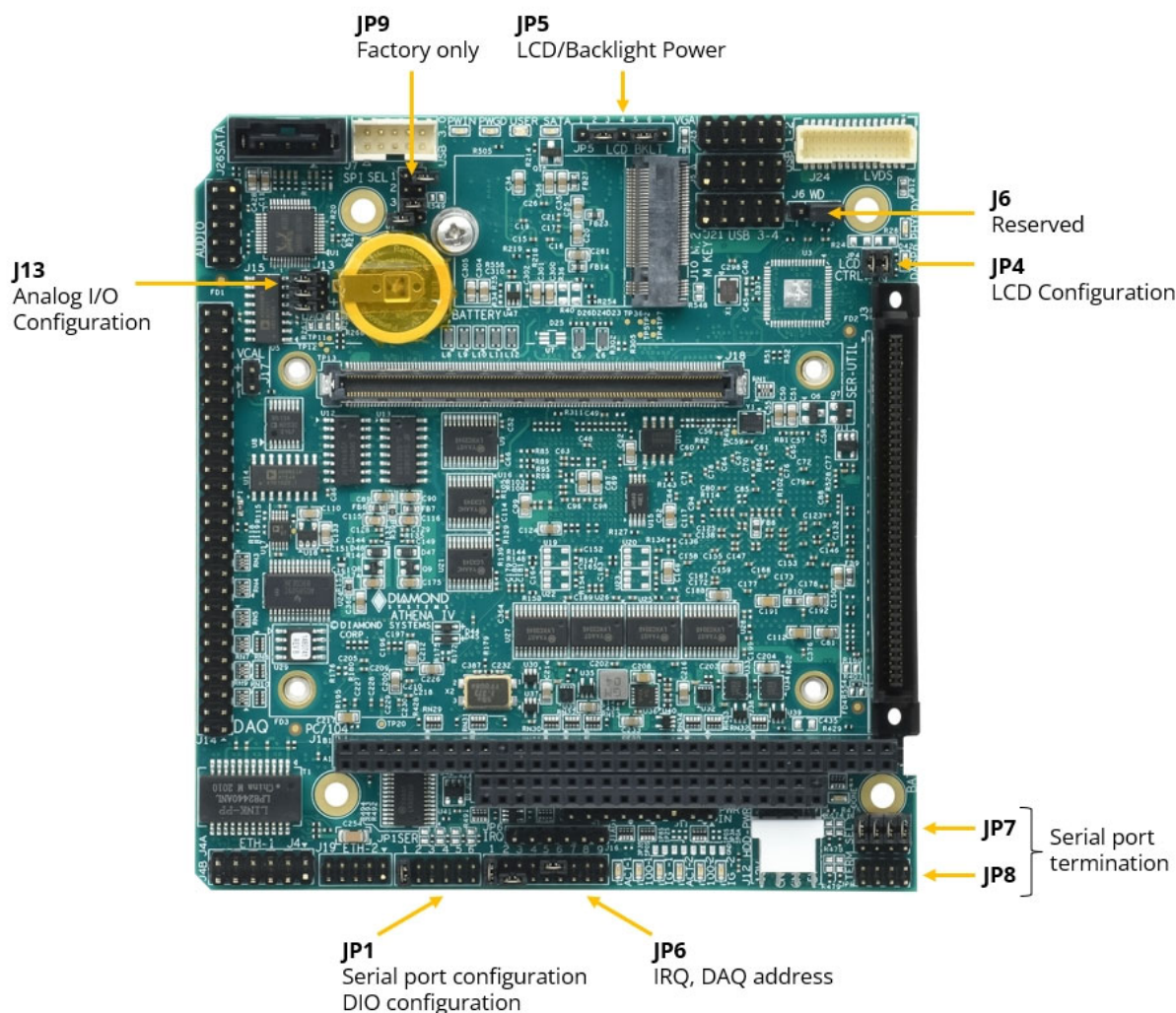


Figure 11-1: Athena IV Jumper Locations

11.2. Connector Reference Table

<i>Connector</i>	<i>Function</i>
J11	Power in
J12	HDD Power output
J5, J21	USB 2.0 (x2)
J7	USB 3.0
J26	SATA
J4	Ethernet-1
J19	Ethernet-2
J25	VGA
J16	JTAG
J24	LVDS
J8 (Bottom side)	LVDS Backlight
J9	External battery
J3	Serial, Utility
J14	DAQ
J15	Audio
J1, J2	PC/104 ISA
J10	M.2
J18	Type 10 COM Express Mini

11.3. Jumper Selection

Athena IV provides ten jumper blocks. The table below summarizes them; the sections that follow describe each user-configurable block in detail. Pin 1 of each block is marked on the board silkscreen.

<i>Block</i>	<i>Size</i>	<i>Function</i>
JP1	2x6, 2 mm	Serial port protocol and DIO pull-up / pull-down
JP4	2x2, 2 mm	LCD scan direction and color mapping
JP5	1x7, 2 mm	LCD panel and backlight voltage
JP6	2x9, 0.1 in	Serial port and A/D interrupt selection
JP7	2x4, 0.1 in	Serial port termination, COM 1 and COM 2
JP8	2x4, 0.1 in	Serial port termination, COM 3 and COM 4
J13	2x3, 2 mm	Data acquisition circuit configuration
J6	1x3, 0.1 in	Reserved
J17	1x2, 0.1 in	Factory use only
JP9	2x4, 0.1 in	Factory use only

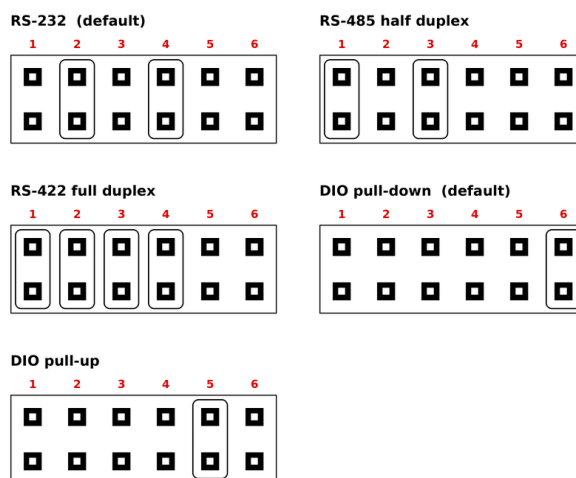
11.3.1. JP1 — Serial Port Protocol and DIO Pull Configuration

JP1 selects the electrical protocol for the four serial ports and the pull resistor applied to the digital I/O lines. The serial ports are configured in pairs: pins 1-2 and 3-4 set the protocol for COM 1 and COM 2 together, and pins 5-6 and 7-8 set it for COM 3 and COM 4 together. Two jumpers are used to select one of the three available protocols.

Protocol	1-2	3-4	5-6	7-8
RS-232 (default)	Out	In	Out	In
RS-485 half duplex	In	Out	In	Out
RS-422 full duplex	In	In	In	In

Pins 9-10 and 11-12 select the pull resistor on the digital I/O lines. Install one jumper only; installing both is not a valid configuration.

Pins	Function
9-10	DIO pull-up enabled
11-12	DIO pull-down enabled (default)

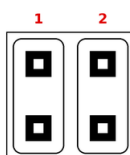


JP1 jumper settings

11.3.2. JP4 — LCD Configuration

JP4 configures the LVDS panel interface. Both settings depend on the panel used; refer to the panel data sheet.

Pins	Function	Installed	Removed
1-2	Scan direction	Normal (default)	Reverse
3-4	Color mapping	Map A (default)	Map B



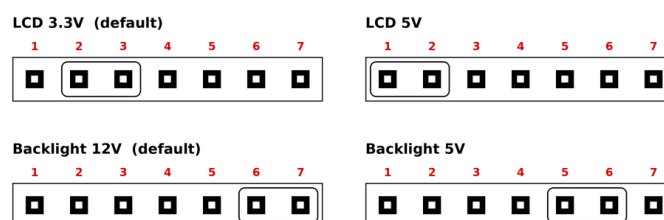
JP4 default settings

11.3.3. JP5 — LCD Panel and Backlight Voltage

JP5 selects the supply voltage for the LVDS panel and for the panel backlight. The two selections are independent. Install one jumper in each group.

Group	Pins	Voltage
LCD panel	1-2	5V
	2-3	3.3V (default)
Backlight	5-6	5V
	6-7	12V (default)

Athena IV does not generate 12V. If the backlight is set to 12V, that voltage must be supplied to the board on the power input connector J11. 12V is likewise only present on the power output connector J12 if it is supplied on J11.

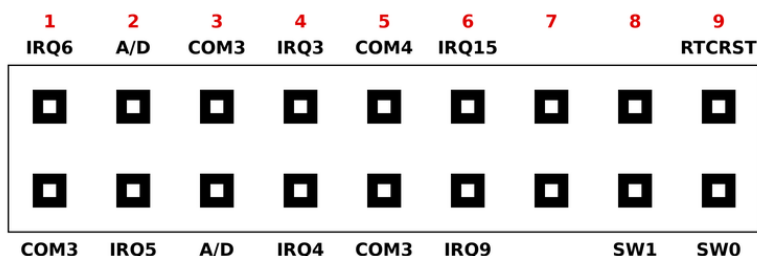


JP5 jumper settings

11.3.4. JP6 — Interrupt Selection, FPGA address

JP6 routes the COM 3, COM 4 and A/D interrupt signals onto the PC/104 bus interrupt lines. Each of the three sources appears on more than one pin of the block, and each PC/104 interrupt line appears on one pin. A jumper connects a source pin to an interrupt pin. Jumpers may be installed horizontally between two adjacent pins in the same row, or vertically across a column.

As illustrated below and as viewed on the board, the left 6 positions numbered 1-6 are used for interrupt configuration. The 3 rightmost positions labeled 7-9 are reserved and should not be used.



JP6 pin assignments

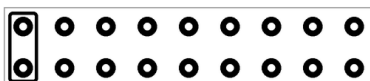
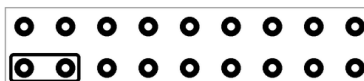
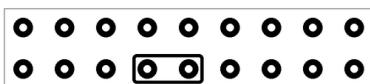
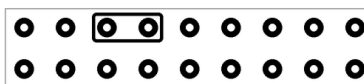
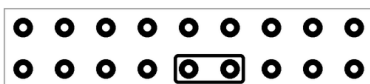
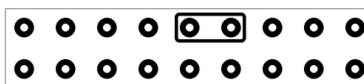
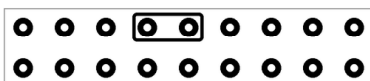
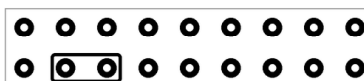
The table below lists the interrupt lines available to each source.

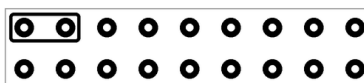
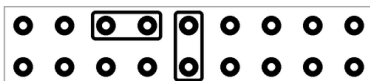
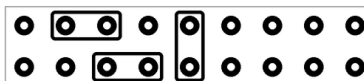
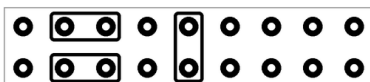
Device	IRQ3	IRQ4	IRQ5	IRQ6	IRQ9	IRQ15
COM3	Yes	Yes	Yes	Default	Yes	-
COM4	Yes	-	-	-	-	Default
A/D	-	Yes	Default	Yes	-	-

Jumper positions are as follows.

Device	IRQ	Jumper position
COM3	6	1, both rows (default)
COM3	5	1-2, lower row
COM3	4	4-5, lower row
COM3	9	5-6, lower row
COM3	3	3-4, upper row
COM4	15	5-6, upper row (default)
COM4	3	4-5, upper row
A/D	5	2-3, lower row (default)
A/D	4	3-4, lower row
A/D	6	1-2, upper row

Two or three sources may share a single interrupt line. This is done by connecting the sources to each other as well as to the interrupt line. The vertical position at pins 9-10 connects COM 4 to COM 3, and the position at pins 13-15 connects COM 3 to A/D.

COM3: IRQ6 (default)

COM3: IRQ5

COM3: IRQ4

COM3: IRQ3

COM3: IRQ9

COM4: IRQ15 (default)

COM4: IRQ3

A/D: IRQ5 (default)

A/D: IRQ4

A/D: IRQ6

COM3, COM4: IRQ3

COM3, COM4, A/D: IRQ4

COM3, COM4, A/D: IRQ5


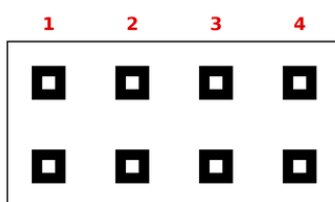
JP6 jumper setting examples (not a complete list of all options)

11.3.5. JP7 and JP8 — Serial Port Termination

JP7 and JP8 connect a 120 ohm termination resistor across the indicated differential signal pair. Termination applies only when a port is configured for RS-422 or RS-485 operation. The default configuration is RS-232 on all ports, so no jumpers are installed.

On a multidrop RS-485 bus, termination should be installed only at the two ends of the bus, not at every node.

<i>Pins</i>	<i>JP7</i>	<i>JP8</i>
1-2	TX1 termination	TX3 termination
3-4	RX1 termination	RX3 termination
5-6	TX2 termination	TX4 termination
7-8	RX2 termination	RX4 termination



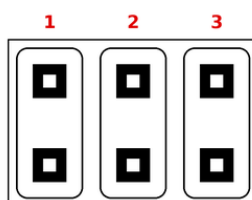
JP7 and JP8 pin assignments

11.3.6. J13 — Data Acquisition Configuration

J13 configures the analog input mode and polarity, and the state to which the analog outputs are set on reset.

<i>Pins</i>	<i>Function</i>	<i>Installed</i>	<i>Removed</i>
1-2	A/D input mode	Single-ended (default)	Differential
3-4	A/D input polarity	Unipolar (default)	Bipolar
5-6	D/A clear mode	Clear to 000h (default)	Clear to 800h

The D/A clear mode selects the code the analog outputs are set to when the D/A is cleared. Code 000h is the bottom of the output range and is used with unipolar ranges such as 0-5V, so that the outputs clear to 0V. Code 800h is the middle of the output range and is used with bipolar ranges such as +/-5V, so that the outputs again clear to 0V.



J13 default settings

11.3.7. Factory Use Only

The following blocks are used during manufacturing and calibration. They are set correctly before shipment and should not be changed. J6 is reserved.

<i>Block</i>	<i>Purpose</i>
J6	Reserved
J17	Data acquisition circuit calibration
JP9	FPGA flash programming control

12. I/O Connector Pinouts

12.1. Power In (J11)

Athena IV provides 1x9 pin header for power input.

1	+5V In
2	Ground
3	Ground
4	+12V In (Optional)
5	Ground
6	+5V In
7	-12VIn (Optional)
8	-5VIn (Optional)
9	PS_ON

Connector Type: 1x9 Header ST Through Hole; PRPC040SAAN-RC-6 from Sullins Connector is used

Mating cable: 698009

12.2. HDD Power Output (J12)

This connector supplies power to an external drive attached to the SATA connector.

1	+5V In
2	Ground
3	Ground
4	+12V

Connector Type: 1x4 Connector RA Through Hole; 640457-4 from TE Connectivity is used

Mating cable: 6981006

12.3. External Battery (J9)

1	Battery +
2	Ground

An external battery may be connected externally to support real-time clock.

Connector Type: Tyco 640457-2 right-angle friction lock pin header

Mating cable: 6981011

12.4. Ethernet 10/100/1000 Port-1 (J4)

Athena IV provides two Gigabit Ethernet port. The pinout of first Ethernet connector is assigned such that, the left column matches the 10/100 Ethernet pinout on Athena II (J4A), for backward compatibility with existing Athena II mating cables and applications. For Gigabit operation all 12 pins are used.

NC	1	2	Key
DB-	3	4	DC-
NC	5	6	DC+
DB+	7	8	NC
DA-	9	10	DD-
DA+	11	12	DD+

Connector Type: Standard 2.54mm dual row straight pin header with gold flash plating

Mating cable: DSC no. **6981086** (gigabit Ethernet) / Alternative: DSC no. **C-PRZ-02** (10/100 Ethernet, 6 pins)

12.5. Ethernet 10/100/1000 Port-2 (J19)

2nd Ethernet port supports Gigabit Ethernet with DSC standard Gigabit Ethernet pinouts

Shield	1	2	Key
DA+	3	4	DA-
DB+	5	6	DB-
DC+	7	8	DC-
DD+	9	10	DD-

Connector Type: Standard 2mm dual row straight pin header with gold flash plating

Mating cable: DSC no. **6981080**

12.6. USB 2.0 Ports (J5, J21)

There are two USB2.0 connectors with identical pinouts. Each connector provides access to two USB 2.0 ports.

Key	1	2	Shield
GND	3	4	GND
USB1/3 Data+	5	6	USB0/2 Data+
USB1/3 Data-	7	8	USB0/2 Data-
USB1/3 VCC+	9	10	USB0/2 VCC

Connector type: Standard 2.54mm dual row straight pin header with gold flash plating will be used.

The shield pin is tied to system ground. The Key pin is cut.

12.7. USB 3.0 Port (J7)

Athena IV supports 1x USB3.0 interface from the COM.

SSRX-	1	2	Shield
SSRX+	3	4	GND
GND	5	6	USB2 Data+
SSTX-	7	8	USB2 Data-
SSTX+	9	10	USB3 VCC

Connector Type: Vertical 2mm, 2x5 dual row through hole connector.

Mating cable: 6980603

12.8. Serial Port Connector (J3)

An 80-pin high-density connector is provided for access to legacy I/O plus miscellaneous functions.

	Pin	RS-232	RS-422	RS-485
COM 1	1	NC	NC	NC
	2	NC	NC	NC
	3	RXD 1	TXD+	TXD/RXD+
	4	RTS 1	TXD-	TXD/RXD-
	5	TXD 1	Ground	Ground
	6	CTS 1	RXD-	NC
	7	NC	RXD+	NC
	8	NC	NC	NC
	9	Ground	Ground	Ground
COM 2	10	NC	NC	NC
	11	NC	NC	NC
	12	RXD 2	TXD+	TXD/RXD+
	13	RTS 2	TXD-	TXD/RXD-
	14	TXD 2	Ground	Ground
	15	CTS 2	RXD-	NC
	16	NC	RXD+	NC
	17	NC	NC	NC
	18	Ground	Ground	Ground
COM 3	19	NC	NC	NC
	20	NC	NC	NC
	21	RXD 3	TXD+	TXD/RXD+
	22	RTS 3	TXD-	TXD/RXD-
	23	TXD 3	Ground	Ground
	24	CTS 3	RXD-	NC
	25	NC	RXD+	NC
	26	NC	NC	NC
	27	Ground	Ground	Ground
COM 4	28	[PWR_BTN*]	[PWR_BTN*]	[PWR_BTN*]
	29	[RST*]	[RST*]	[RST*]
	30	RXD 4	TXD+	TXD/RXD+
	31	RTS 4	TXD-	TXD/RXD-
	32	TXD 4	Ground	Ground
	33	CTS 4	RXD-	NC
	34	I2C CLK	I2C CLK	I2C CLK
	35	I2C Data	I2C Data	I2C Data
	36	Ground	Ground	Ground
Utilities	37	+5V Out	+5V Out	+5V Out
	38	Speaker Out	Speaker Out	Speaker Out
	39	SATA LED	SATA LED	SATA LED
	40	Power LED	Power LED	Power LED

COM 1 through COM 4 signal assignments depend on the protocol selected with JP1. All three protocols are shown above.

Connector Type: PCB footprint is compatible with 3M P50E-080P1-S1-EA “regular density”

Mating cable: DSC no. **6981014**

12.9. VGA (J25)

Standard 2.54mm dual row straight pin header with gold flash plating will be used as VGA connector.

Ground	1	2	Ground
Green	3	4	Red
Blue	5	6	Ground
HSync	7	8	DDC-Data
VSynC	9	10	DDC-Clock

Connector type: Standard 2.54mm dual row straight pin header with gold flash plating.

Mating cable: DSC no. **6981030**

12.10. LVDS (J24)

The LCD panel power is jumper-selectable for 3.3V (default) or 5V.

Ground	1	2	Ground
LVDS clock-	3	4	
LVDS clock+	5	6	
Ground	7	8	Ground
LVDS data 0--	9	10	LVDS data 3+
LVDS data 0+	11	12	LVDS data 3-
Ground	13	14	Ground
LVDS data 2--	15	16	
LVDS data 2+	17	18	
Ground	19	20	Ground
LVDS data 1+	21	22	Scan Direction
LVDS data 1-	23	24	LVDS Map
Ground	25	26	Ground
VDD (LCD Display)	27	28	VDD (LCD Display)
VDD (LCD Display)	29	30	VDD (LCD Display)

Connector Type: JST model no. BM30B-SRDS-G-TF

Mating cable connector: Connector: JST model no. SHDR-30V-S-B

Terminals: JST model no. SSH-003GA-P0.2

Mating cable: Customer assembly required

12.11. LCD Backlight (J8)

The brightness control for the LCD backlight has a weak pull-down resistor to ensure maximum brightness when it is not connected externally. This signal may be controlled by a GPIO pin on the CPU through PWM. A jumper selects the source of the brightness signal to this pin.

1	Power +5V/+12V, jumper selectable
2	Power (same as pin 1)
3	Ground
4	Ground
5	Enable (GPIO output), 0 = off, open circuit = on
6	Brightness, 0-5VDC variable; 0V = max, 5V = min

Connector Type: Molex 53047-0610 pin VERT 1.25mm pitch TH header.

Mating cable: 6981216

Mating Cable Connector: **Socket:** Molex 51021-0600 or equivalent
Terminals: Molex 50058 / 50079 series or equivalent

12.12. Audio (J15)

This connector provides the audio signals.

Line Out Left	1	2	Line Out Right
Ground	3	4	Line In left
Line In Right	5	6	Ground
Mic In	7	8	NC
Key	9	10	Ground

Connector Type: Standard 2x5 2.54mm dual row straight pin header with gold flash

Mating cable: 6981031

12.13. Data Acquisition I/O Connector (J14)

Athena IV includes a 50-pin header for all data acquisition I/O. This header is located on the left side of the board. Pin 1 is the lower right pin and is marked on the board.

DIO A0	1	2	DIO A1
DIO A2	3	4	DIO A3
DIO A4	5	6	DIO A5
DIO A6	7	8	DIO A7
DIO B0	9	10	DIO B1
DIO B2	11	12	DIO B3
DIO B4	13	14	DIO B5
DIO B6	15	16	DIO B7
DIO C0	17	18	DIO C1
DIO C2	19	20	DIO C3
DIO C4 / Gate 0	21	22	DIO C5 / Gate 1
DIO C6 / Clk 1	23	24	DIO C7 / Out 0
Ext Trig	25	26	Tout 1
+5V Out	27	28	Dground
Vout 0	29	30	Vout 1
Vout 2	31	32	Vout 3
Aground (Vout)	33	34	Aground (Vin)
Vin 0	35	36	Vin 8
Vin 1	37	38	Vin 9
Vin 2	39	40	Vin 10
Vin 3	41	42	Vin 11
Vin 4	43	44	Vin 12
Vin 5	45	46	Vin 13
Vin 6	47	48	Vin 14
Vin 7	49	50	Vin 15

Connector Type: Standard .1" single row straight pin header with gold flash plating

Mating cable: C-50-18

12.16. COM Express Type 10 (J18)

GND	A1	B1	GND	EXCD0_CPPE#	A49	B49	SYS_RESET#
GBE0_MDI3-	A2	B2	GBE0_ACT#	LPC_SERIRQ	A50	B50	CB_RESET#
GBE0_MDI3+	A3	B3	LPC_FRAME#	GND	A51	B51	GND
GBE0_LINK100#	A4	B4	LPC_AD0	RSVD (N/C)	A52	B52	RSVD (N/C)
GBE0_LINK1000#	A5	B5	LPC_AD1	RSVD (N/C)	A53	B53	RSVD (N/C)
GBE0_MDI2-	A6	B6	LPC_AD2	SD_DATA0	A54	B54	SD_CMD
GBE0_MDI2+	A7	B7	LPC_AD3	RSVD (N/C)	A55	B55	RSVD (N/C)
GBE0_LINK# (N/C)	A8	B8	LPC_DRQ0#(N/C)	RSVD (N/C)	A56	B56	RSVD (N/C)
GBE0_MDI1-	A9	B9	LPC_DRQ1# (N/C)	GND	A57	B57	SD_WP
GBE0_MDI1+	A10	B10	LPC_CLK	PCIE_TX3+ (N/C)	A58	B58	PCIE_RX3+ (N/C)
GND	A11	B11	GND	PCIE_TX3- (N/C)	A59	B59	PCIE_RX3- (N/C)
GBE0_MDI0-	A12	B12	PWRBTN#	GND	A60	B60	GND
GBE0_MDI0+	A13	B13	SMB_CK	PCIE_TX2+	A61	B61	PCIE_RX2+
GBE0_CTREF (N/C)	A14	B14	SMB_DAT	PCIE_TX2-	A62	B62	PCIE_RX2-
SUS_S3#	A15	B15	SMB_ALERT#	SD_DATA1	A63	B63	SD_CD#
SATA0_TX+	A16	B16	SATA1_TX+	PCIE_TX1+	A64	B64	PCIE_RX1+
SATA0_TX-	A17	B17	SATA1_TX-	PCIE_TX1-	A65	B65	PCIE_RX1-
SUS_S4#	A18	B18	SUS_STAT#	GND	A66	B66	WAKE0#
SATA0_RX+	A19	B19	SATA1_RX+	SD_DATA2	A67	B67	WAKE1#
SATA0_RX-	A20	B20	SATA1_RX-	PCIE_TX0+	A68	B68	PCIE_RX0+
GND	A21	B21	GND	PCIE_TX0-	A69	B69	PCIE_RX0-
USB_SSRX0-	A22	B22	USB_SSTX0-	GND	A70	B70	GND
USB_SSRX0+	A23	B23	USB_SSTX0+	LVDS_A0+	A71	B71	DDIO_PAIR0+
SUS_S5#	A24	B24	PWR_OK	LVDS_A0-	A72	B72	DDIO_PAIR0-
USB_SSRX1- (N/C)	A25	B25	USB_SSTX1- (N/C)	LVDS_A1+	A73	B73	DDIO_PAIR1+
USB_SSRX1+ (N/C)	A26	B26	USB_SSTX1+ (N/C)	LVDS_A1-	A74	B74	DDIO_PAIR1-
BATLOW#	A27	B27	WDT (N/C)	LVDS_A2+	A75	B75	DDIO_PAIR2+
ATA_ACT#	A28	B28	AC_SDIN2 (N/C)	LVDS_A2-	A76	B76	DDIO_PAIR2-
AC_SYNC	A29	B29	AC_SDIN1	LVDS_VDD_EN	A77	B77	DDIO_PAIR4+ (N/C)
AC_RST#	A30	B30	AC_SDIN0	LVDS_A3+	A78	B78	DDIO_PAIR4- (N/C)
GND	A31	B31	GND	LVDS_A3-	A79	B79	LVDS_BKLT_EN
AC_BITCLK	A32	B32	SPKR	GND	A80	B80	GND
AC_SDOUT	A33	B33	I2C_CK	LVDS_A_CLK+	A81	B81	DDIO_PAIR3+
BIOS_DIS0#	A34	B34	I2C_DAT	LVDS_A_CLK-	A82	B82	DDIO_PAIR3-
THRMTRIP#	A35	B35	THRM#	LVDS_I2C_CK	A83	B83	LVDS_BKLT_CTRL
USB6-	A36	B36	USB7-	LVDS_I2C_DAT	A84	B84	VCC_5V_SBY
USB6+	A37	B37	USB7+	SD_DATA3	A85	B85	VCC_5V_SBY
USB_6_7_OC# (N/C)	A38	B38	USB_4_5_OC# (N/C)	RSVD (N/C)	A86	B86	VCC_5V_SBY
USB4-	A39	B39	USB5-	RSVD	A87	B87	VCC_5V_SBY
USB4+	A40	B40	USB5+	PCIE0_CK_REF+	A88	B88	BIOS_DIS1#
GND	A41	B41	GND	PCIE0_CK_REF-	A89	B89	DDIO_HPD
USB2-	A42	B42	USB3-	GND	A90	B90	GND
USB2+	A43	B43	USB3+	SPI_POWER	A91	B91	DDIO_PAIR5+ (N/C)
USB_2_3_OC# (N/C)	A44	B44	USB_0_1_OC# (N/C)	SPI_MSIO	A92	B92	DDIO_PAIR5- (N/C)
USB0-	A45	B45	USB1-	SD_CLK	A93	B93	DDIO_PAIR6+ (N/C)
USB0+	A46	B46	USB1+	SPI_CKL	A94	B94	DDIO_PAIR6- (N/C)
VCC_RTC	A47	B47	EXCD1_PERST#	SPI_MOSI	A95	B95	DDIO_DDC_AUX_SEL
EXCD0_PERST#	A48	B48	EXCD1_CPPE#	TPM_PP (N/C)	A96	B96	USB_HOST_PRST (N/C)

TYPE10#	A97	B97	SPI_CS#
SER0_TX	A98	B98	DDIO_CTRLCLK_AUX+
SER0_RX	A99	B99	DDIO_CTRLCLK_AUX-
GND	A100	B100	GND
SER1_TX (N/C)	A101	B101	FAN_PWMOUT(N/C)
SER1_RX (N/C)	A102	B102	FAN_TACHIN(N/C)
LID#	A103	B103	SLEEP#

VCC_5V	A104	B104	VCC_5V
VCC_5V	A105	B105	VCC_5V
VCC_5V	A106	B106	VCC_5V
VCC_5V	A107	B107	VCC_5V
VCC_5V	A108	B108	VCC_5V
VCC_5V	A109	B109	VCC_5V
GND	A110	B110	GND

12.17. PC/104 Bus Connectors (J1, J2)

The PC/104 bus is essentially identical to the ISA Bus except for the physical design. It specifies two pin and socket connectors for the bus signals. A 64-pin header incorporates the 62-pin 8-bit bus connector signals, and a 40-pin header incorporates the 36-pin 16-bit bus connector signals. View from top of board.

PC/104 16-bit bus connector

Ground	D0	C0	Ground
MEMCS16-	D1	C1	SBHE-
IOCS16-	D2	C2	LA23
IRQ10	D3	C3	LA22
IRQ11	D4	C4	LA21
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
DACK0-	D8	C8	LA17
DRQ0	D9	C9	MEMR-
DACK5-	D10	C10	MEMW-
DRQ5	D11	C11	SD8
DACK6-	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7-	D14	C14	SD11
DRQ7	D15	C15	SD12
+5V	D16	C16	SD13
MASTER-	D17	C17	SD14
Ground	D18	C18	SD15
Ground	D19	C19	Key (pin cut)

PC/104 8-bit bus connector

IOCHCHK-	A1	B1	Ground
SD7	A2	B2	RESET
SD6	A3	B3	+5V
SD5	A4	B4	IRQ9
SD4	A5	B5	-5V
SD3	A6	B6	DRQ2
SD2	A7	B7	-12V
SD1	A8	B8	0WS-
SD0	A9	B9	+12V
IOCHRDY	A10	B10	Key (pin cut)
AEN	A11	B11	SMEMW-
SA19	A12	B12	SMEMR-
SA18	A13	B13	IOW-
SA17	A14	B14	IOR-
SA16	A15	B15	DACK3-
SA15	A16	B16	DRQ3
SA14	A17	B17	DACK1-
SA13	A18	B18	DRQ1
SA12	A19	B19	Refresh-
SA11	A20	B20	SYSCLK
SA10	A21	B21	IRQ7
SA9	A22	B22	IRQ6
SA8	A23	B23	IRQ5
SA7	A24	B24	IRQ4
SA6	A25	B25	IRQ3
SA5	A26	B26	DACK2-
SA4	A27	B27	TC
SA3	A28	B28	BALE
SA2	A29	B29	+5V
SA1	A30	B30	OSC
SA0	A31	B31	Ground
Ground	A32	B32	Ground

Connector Type: 2x32 PC/104 connector; 962-60323-12, 2x20 PC/104 connector; 962-60203-12

13. Athena IV I/O Connector List & Mating Cables

The following table provides a summary of the I/O connectors on the board.

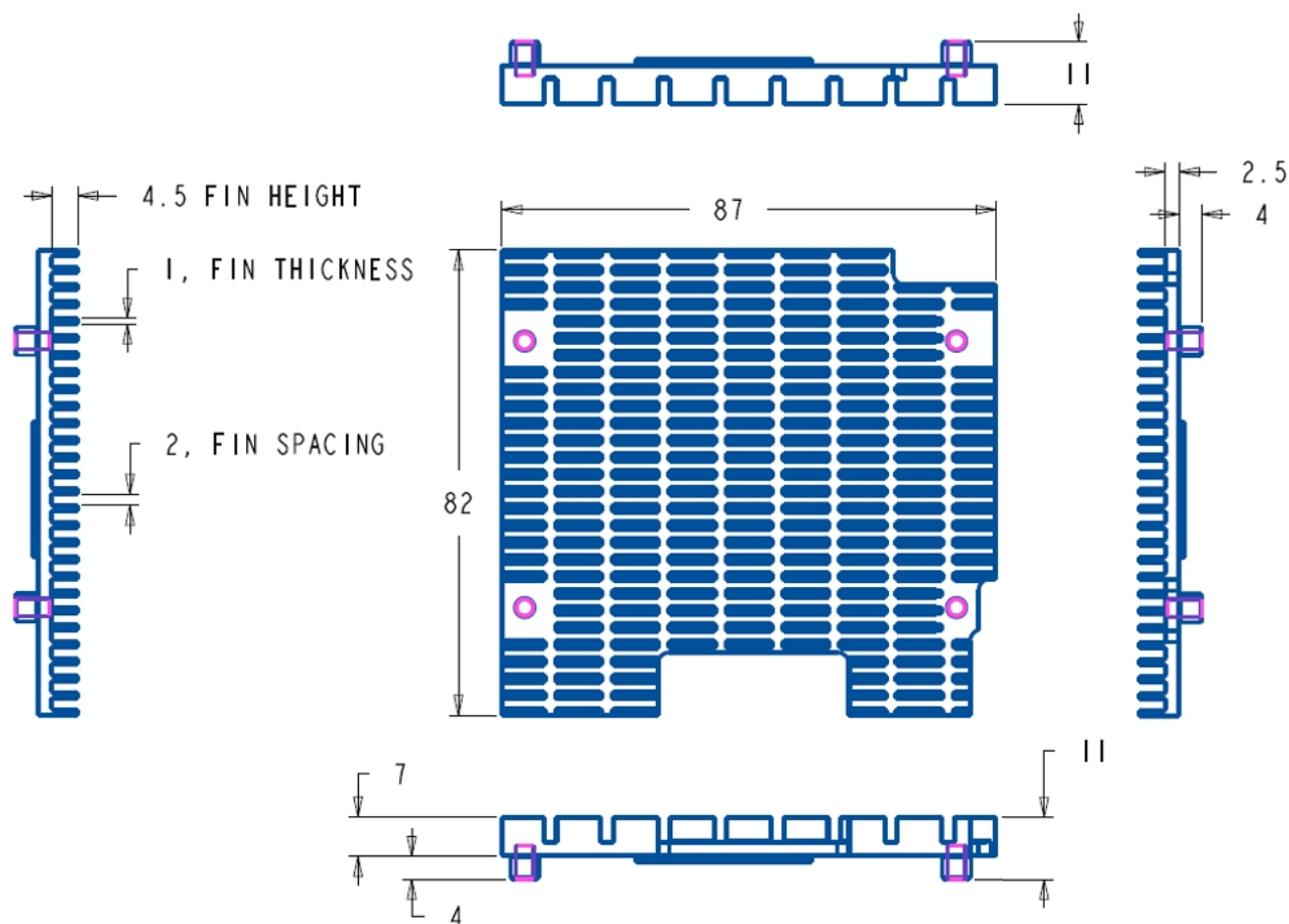
<i>Function</i>	<i>Manufacturer</i>	<i>Part no.</i>	<i>Description</i>	<i>DSC Mating Cable</i>
Power in	Sullins Connector	PRPC040SAAN-RC-6	CONN HEADER VERT 9POS 2.54MM	698009
HDD Power output	TE Connectivity	640457-4	CONN HEADER R/A 4POS 2.54MM	6981006
USB 2.0 (x2)	Oupiin	2011-2X40G00SD025/SN	2x5, 2.54mm pitch, TH header	6981012
USB 3.0	Amphenol	9814-G06-10ULF	10 Position 2mm vertical connector	6980603
Ethernet-1	Harwin	M20-9980645	2x6, 2.54mm pitch, TH header	C-PRZ-02 (100 Mbps)
Ethernet-2	Pinrex	220-9205GB01	2x5, 2mm pitch, TH header	6981080
VGA	Oupiin	2011-2X40G00SD025/SN	2x5, 2.54mm pitch, TH header	6981030
JTAG	Aptos	LHY-06S-VB-060/030-FG	1x6, 2.54mm pitch, TH header	N/A
LVDS	JST	BM30B-SRDS-G-TF(LF)(SN)	CONN HEADER SHD 30POS TOP 1MM	N/A
Backlight	Molex	053261-0671	6POS RA TH	6981216
External battery	TYC	640457-2	CONN HEADER RTANG 2POS .100 TIN	6981011
Serial Port	3M	P50E080P1-S1-EA	Conn PL 40 POS 2.54mm Solder ST TH	C-PRZ-01
DAQ	Oupiin	2011-2X40G00SD025/SN	2x25, 2.54mm pitch, TH header	C-50-18
Audio	Oupiin	2011-2X40G00SD025/SN	2x5, 2.54mm pitch, TH header	6981031
M.2	Amphenol	MDT420M03001	CONN FEMALE 67POS 0.020 GOLD	NA
SATA	Molex	67800-8025	CONN HEADER 7POS VERT T/H	Standard Cable
PC/104 ISA	EPT	962-60323-12 962-60203-12	CONN PC/104 32POS TH VERT CONN PC/104 20POS TH VERT	NA
Type 10 COM Express Mini	Foxconn	QT002206-4131-3H	220 Position Connector Plug, SMT, Outer Shroud Contacts Surface Mount Gold	NA

14. Heat Sink

The heat sink is a custom shaped single piece of aluminum with a clear finish, with a form factor of 3.42" x 3.22". This size is larger than the COM module itself, which enables more efficient heat dissipation.

To enable improved heat dissipation and high temperature reliability, the heat sink is extended over the top side of the PC104 connectors, preventing installation of PC/104 I/O modules above the board. Athena IV supports bottom side PC/104 I/O modules only.

The notch in the bottom edge of the illustration provides clearance for installation of a M.2 2230 flashdisk.



Athena IV heat sink

15. Specifications

The specifications of Athena IV are tabulated below:

Feature	Description
CPU	Intel® Atom™ processor WT E3940/E3950 COM Express Type 10 CPU module
Cooling Accessory	Passive heat sink
Memory	4/8 GB
Display	1x VGA 1x 24-bit Single Channel LVDS Display
USB Ports	4x USB 2.0 1x USB 3.0
	4 RS-232/422/485 Ports. Max data rate 1Mbps (115200 baud rate)
Serial Ports	RS232 voltage specification: +/-6.6Vaa RS485/RS422 Driver Common mode voltage is 3V RS485/RS422 Driver differential voltage is 1.5 to 3V
Ethernet Controller	ETH-1 10/100/1000Mbps Routed from CoM Module ETH-2 10/100/1000Mbps Routed from Intel I210 Ethernet Controller
	1x SATA for standard 7-pin hard drives
Mass Storage	1x M.2 SATA Socket 2230 (22mm Wide x 30mm Long) 1x eMMC of 64/128 GB (available only on E3940/E3950 models)
Expansion Bus	1x PC/104 bus supporting 8-bit & 16-bit transactions with interrupts Default Setting
ISA Resource	ISA Address - 0x280 ISA IRQ - 5
Utility	1x I2C, Power Button, Reset Button, +5V 1x Speaker out. Connect a speaker between this pin and +5V Out

DAQ Specifications

Feature	Description
ADC	
Number of channels	8x Single Ended or
	16x Differential Ended
Resolution	16-bit
Input Voltage Range	Unipolar Range: 0-10V, 0-5V, 0-2.5V, 0-1.25V
	Bipolar Range: $\pm 10V$, $\pm 5V$, $\pm 2.5V$, $\pm 1.25V$
Calibration	Auto calibration
DAC	
Number of channels	4
Resolution	12-bits
Output Mode	Unipolar Range: 0-10V
	Bipolar Range: $\pm 10V$
Calibration	Auto calibration
Digital I/O	
Voltage	3.3V output compliant
	5V input tolerant
Number of digital lines	24
Direction	Bidirectional
Programmability	Port A, B: Port Programmable
	Port C: Nibble programmable
Polarity	Active High
Input voltage	Logic 0:
	Low: 1.72 - 0V
	Logic 1
	High: 1.76 - 5.5V
Output Voltage	Logic 0:
	Low: 0.55 - 0V @ 24mA
	Logic 1
	High: 2.2 - 3.3V @ -24mA

Mechanical and Environmental Properties

Feature	Description
Dimensions	L 4.475" x W 3.975" (113.6 mm x 100.9 mm)
Weight	TBU With/Without Heat Spreader
DC Power Input Voltage	Main power input: 5VDC LVDS Backlight: 5/12V (Display dependent)
Power Consumption	8.5 W (Typical) 16 W (Stress)*
Operating Temperature	-40°C to +85°C (-40°F to +185°F)
Shock	MIL-STD-202G Compatible
Vibration	MIL-STD-202G Compatible
RoHS	Compliant

*:- Stress conditions are

VGA connected, 3 USB devices connected, 1 GbE connected, No add on modules, M.2 SATA HDD, in Win 10 OS, Intel Diagnosis Tool with load as CPU100% and GFX 100%, BurnIn Test (all 100%) – 2D, 3D Graphics, Disk, RAM, Network, Sound, Video playback

16. Getting Started

16.1. Software Setup

In order to use Athena IV, an operating system needs to be installed. This OS can be either installed in the M.2 SSD or an external HDD. Depending upon the purchase made, an M.2 SSD may or may not be included with the purchase kit.

The software setup is as described below:

- Download the necessary OS on a workstation. It is recommended to download the OS in ISO format.
- Download the Rufus utility program to create a bootable USB flash disk. Rufus can be downloaded here: [Rufus](#)
- Insert a USB flash disk in the workstation & launch Rufus
- Follow the Rufus settings & initiate the bootable USB flash disk creation process

16.2. Hardware Setup

The illustration below shows the minimum hardware set up required to boot the system:

- Use the cable DSC# 6981012 at J5/J21 and connect a USB mouse & keyboard to the ports.
- Use the cable DSC# 6981030 at J25 & connect a VGA monitor to the port. Make sure to leave out the pins 1 & 2 to connect the cable as these pins are used to enable the system in headless mode (described in [Section 8.9](#)). The VGA signals are available from the pin number 3. See illustration below:
- Connect a SATA HDD at J26 or an M.2 M-Key 2230 sized SSD at J10. The system requires only 1 media to boot. Depending upon availability either one can be connected.
- Connect a 5V power supply at J11.
- Ensure all the connections are in tact.
- Double check the power supply.
- Power on system.
- On the initial boot, the system will prompt for installation settings. Set up as required.
- Once the OS installation is completed, the Desktop is loaded. The system is now ready to be used.