ICS-2000 USER Manual

AMD EPYC™ 8004 Siena Edge AI Server
Expandable, NVIDIA/AMD Full-length Graphics, DC/AC Options

Vecow

1.10 Edition 20260511

Record of Revision

Version	Date	Page	Description	Remark
1.00	2025/12/05	All	Official Release	
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Order Information

Part Number	Description
ICS-2000	AMD EPYC™ 8004 "Siena" Processor Edge AI Server, 2 PCIe x16, 4 PCIe x8, 4 U.2 Tray, DC 16V to 50V
ICS-2000A	AMD EPYC™ 8004 "Siena" Processor Edge AI Server, 2 PCIe x16, 4 PCIe x8, 4 U.2 Tray, AC 90V to 240V

CPU List

Series	Model	Cores	GHz	TDP
EPYC Siena	8224P	24	2.55	160

Optional Accessories

Part Number	Description
DDR5 96G	Certified DDR5 96GB 4800MHz RAM
DDR5 64G	Certified DDR5 64GB 4800MHz RAM
DDR5 32G	Certified DDR5 32GB 4800MHz RAM
DDR5 16G	Certified DDR5 16GB 4800MHz RAM
PWS-1000W-24V	1000W, 24V, 90V AC to 264V AC Power Supply
PWS-1500W-24V	1500W, 24V, 90V AC to 264V AC Power Supply
PWS-3000W-24V	3000W, 24V, 90V AC to 264V AC Power Supply
TMK2-20P-100	Terminal Block 20-pin to Terminal Block 20-pin Cable, 100cm
TMK2-20P-500	Terminal Block 20-pin to Terminal Block 20-pin Cable, 500cm
TMB-TMBK-20P	Terminal Board with One 20-pin Terminal Block Connector and DIN-Rail Mounting
M.2 Storage Module	M.2 Key M Storage Module
U.2 Storage Module	U.2 Storage Module
M.2 to U.2 Module	M.2 to U.2 Module
5G Module	5G Module with Antenna
4G Module	4G/GPS Module with Antenna
WiFi & Bluetooth	WiFi & Bluetooth Module with Antenna

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1

GENERAL INTRODUCTION

1.1 Overview

The Vecow ICS-2000 is a high-performance, server-grade computing platform powered by AMD's 4th Gen EPYC™ 8004 Siena processors. It supports up to 64 cores with a maximum TDP of 255W, making it an ideal solution for demanding edge computing applications. The system accommodates up to six DDR5 4800MHz, delivering a total capacity of 768GB for superior processing efficiency.

Engineered for expandability and connectivity, the ICS-2000 offers six PCIe slots, including two PCIe Gen 5.0 x16 and four PCIe Gen 5.0 x8 slots. Its versatile I/O options include two GigE LAN ports, one management LAN (MLAN) port, two USB ports, and four COM ports, ensuring seamless integration into diverse industrial environments.

For storage, the ICS-2000 features four M.2 slots and four front-access U.2 drive bays, providing ample capacity for high-speed data processing. Its flexible power input design supports both DC (16V–50V) and AC (90V–240V) sources, making it suitable for a wide range of industrial and edge computing deployments.

1.2 Features

- Server-level Platform : AMD EPYC™ 4th Gen 8004 "Siena" Processor, up to 64-core
- 6 DDR5 4800MHz Memory supports up to 768GB
- 2 PCIe 5.0 x16 slots with a total 1800W power budget, supporting up to dual 900W NVIDIA® or AMD 2-slot graphics cards, and 4 PCIe 5.0 x8 slots for expansion cards
- Multiple storage devices : 4 M.2 Key M and 4 Front-access U.2
- 2 LAN, 2 USB, 5 COM, 16-bit DIO, 5G/WiFi 6/4G/LTE/GPRS/UMTS, and TPM 2.0
- DC 16V to 50V or AC 220V power input options with software ignition control

1.3 Product Specification

1.3.1 Specifications of ICS-2000

System	
Processor	AMD EPYC™ 4th Gen 8004 "Siena" Server Processor
BIOS	AMI
SIO	IT8786E
Memory	6 DDR5 RDIMM 4800MHz, up to 768GB
OS	Windows Server, Linux
I/O Interface	
Serial	• 4 COM RS-232/422/485 • 1 COM RS-232
USB	2 USB 3.2 Gen1
Isolated DIO	16 Isolated DIO: 8 DI, 8 DO
Display	DisplayPort : Up to 1920x 1200 @60Hz
LED	Power, HDD, BMC
SIM Card	3 External Nano SIM Card Socket
Expansion	
PCIe	• 2 PCIe x16 slot with PCIe 5.0 x16 signal • 4 PCIe x16 slot with PCIe 5.0 x8 signal
M.2	• 2 M.2 Key B Socket (3042/3052, PCIex1/USB3.0) with SIM • 1 M.2 Key E Socket (2230, PCIex1)
mini PCIe	• 1 Full size Mini-PCIe socket (PCIex1/USB2) with SIM
Storage	
U.2	4 U.2 front access tray (PCIe x4) *M.2 supported by optional accessory
M.2	4 M.2 Key M (2280, PCIe 4.0 x4)
Ethernet	
LAN 1	Intel® I350 GigE LAN
LAN 2	Intel® I350 GigE LAN
LAN 3	GigE MLAN for management (BMC)
Power	
Power Input	16V to 50V, DC-in
Power Interface	6-pin Terminal Block : V+, V+, V+, V-, V-, V-
Ignition Control	16-mode Software Ignition Control
Remote Switch	3-pin Terminal Block

Others	
TPM	Infineon SLB9670 supports TPM 2.0, SPI Interface
Watchdog Timer	Reset : 1 to 255 sec./min. per step
Smart Management	Wake on LAN supported
HW Monitor	Monitoring temperature, voltages. Auto throttling control when CPU overheats.
Mechanical	
Dimension (W x D x H)	345mm x 405mm x 200mm (13.58" x 15.94" x 7.87")
Weight	13.1Kg (28.88lb)
Mounting	Wallmount by mounting bracket
Environment	
Operating Temperature	-25°C to 45°C
Storage Temperature	-40°C to 85°C (-40°F to 185°F)
Humidity	5% to 95% Humidity, non-condensing
Relative Humidity	95% @45°C
Shock	MIL-STD-810G method 514.6
Vibration	MIL-STD-810G method 516.6
EMC	CE, FCC, EN50155, EN50121-3-2

1.3.2 Specifications of ICS-2000A

System	
Processor	AMD EPYC™ 4th Gen 8004 "Siena" Server Processor
BIOS	AMI
SIO	IT8786E
Memory	6 DDR5 RDIMM 4800MHz, up to 768GB
OS	Windows Server, Linux
I/O Interface	
Serial	• 4 COM RS-232/422/485 • 1 COM RS-232
USB	2 USB 3.2 Gen1
Isolated DIO	16 Isolated DIO: 8 DI, 8 DO
Display	DisplayPort : Up to 1920x 1200 @60Hz
LED	Power, HDD, BMC
SIM Card	3 External Nano SIM Card Socket
Expansion	
PCIe	• 2 PCIe x16 slot with PCIe 5.0 x16 signal • 4 PCIe x16 slot with PCIe 5.0 x8 signal
M.2	• 2 M.2 Key B Socket (3042/3052, PCIex1/USB3.0) with SIM • 1 M.2 Key E Socket (2230, PCIex1)
mini PCIe	• 1 Full size Mini-PCIe socket (PCIex1/USB2) with SIM
Storage	
U.2	4 U.2 front access tray (PCIe x4) *M.2 supported by optional accessory
M.2	4 M.2 Key M (2280, PCIe 4.0 x4)
Ethernet	
LAN 1	Intel® I350 GigE LAN
LAN 2	Intel® I350 GigE LAN
LAN 3	GigE MLAN for management (BMC)
Power	
Power Input	90V to 240V, AC-in (3000W @220V)
Power Interface	3-pin C14-type AC Plug
Ignition Control	16-mode Software Ignition Control
Remote Switch	3-pin Terminal Block

Others	
TPM	Infineon SLB9670 supports TPM 2.0, SPI Interface
Watchdog Timer	Reset : 1 to 255 sec./min. per step
Smart Management	Wake on LAN supported
HW Monitor	Monitoring temperature, voltages. Auto throttling control when CPU overheats.
Mechanical	
Dimension (W x D x H)	345mm x 405mm x 200mm (13.58" x 15.94" x 7.87")
Weight	13.1Kg (28.88lb)
Mounting	Wallmount by mounting bracket
Environment	
Operating Temperature	-5°C to 45°C
Storage Temperature	-20°C to 85°C (-4°F to 185°F)
Humidity	5% to 95% Humidity, non-condensing
Relative Humidity	95% @45°C
Shock	MIL-STD-810G method 514.6
Vibration	MIL-STD-810G method 516.6
EMC	CE, FCC, EN50155, EN50121-3-2

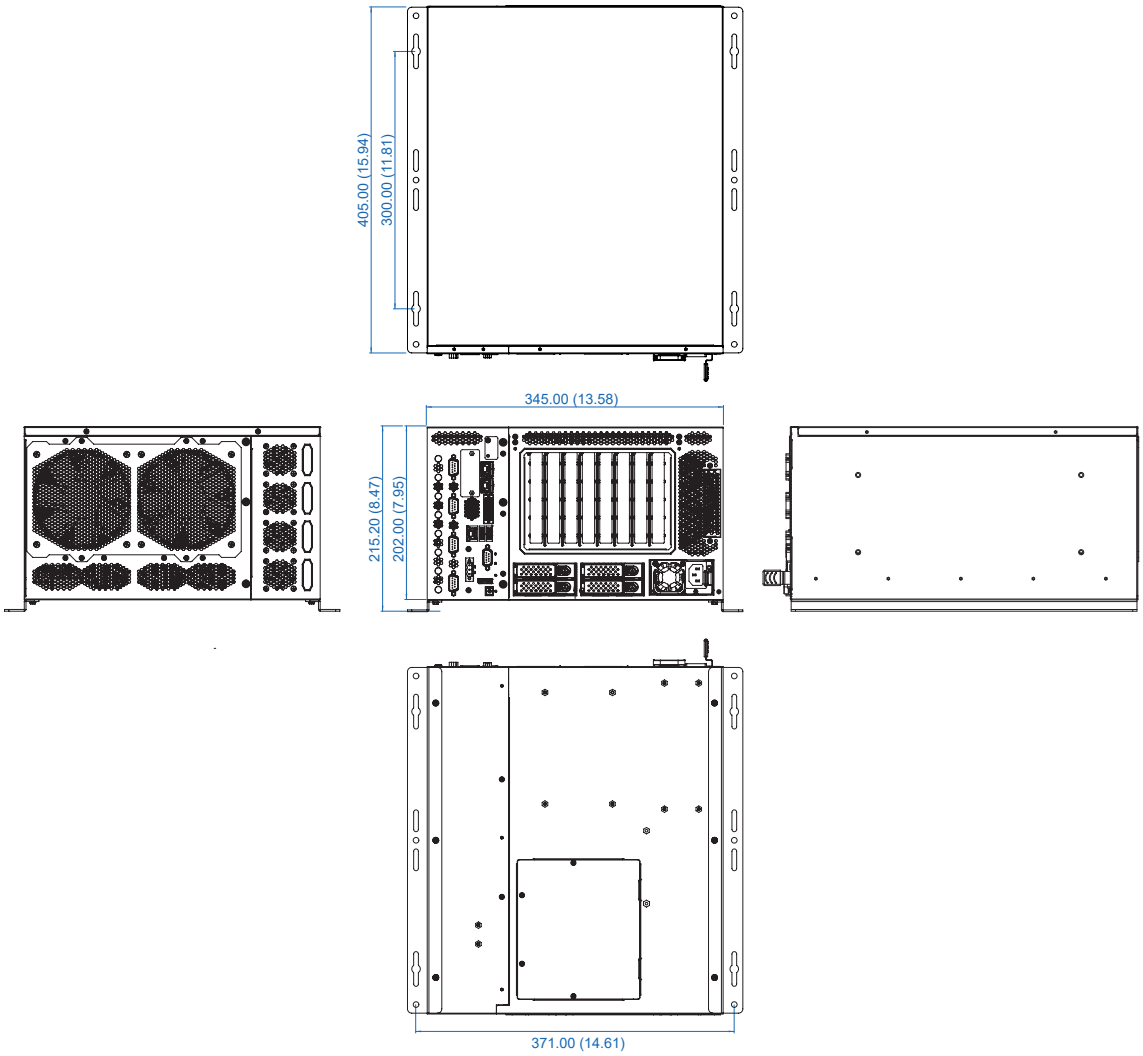
1.4 Supported CPU List

Series	Model	Cores	GHz	TDP
EPYC Siena	8224P	24	2.55	160

1.5 Mechanical Dimension

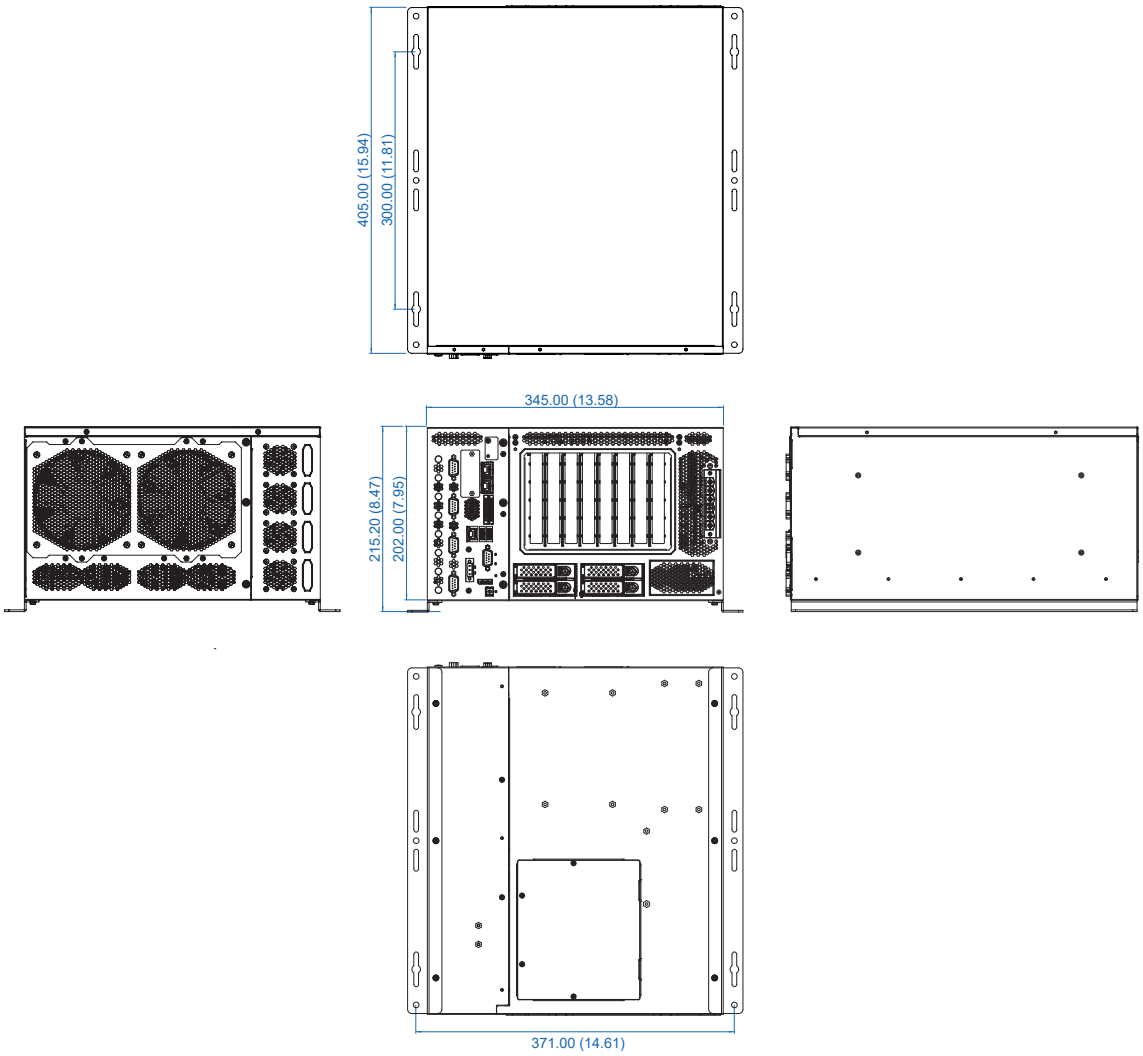
1.5.1 Dimensions of ICS-2000

Unit : mm (inch)



1.5.2 Dimensions of ICS-2000A

Unit : mm (inch)



2

GETTING TO KNOW YOUR ICS-2000

2.1 Packing List

2.1.1 ICS-2000 Packing List

Item	Description	Qty
1	ICS-2000 AI Computing System (According to the configuration you order, the ICS-2000 series may contain SSD and DDR5 R DIMM. Please verify these items if necessary.)	1

Item	Description	Outlook	Usage	P/N	Qty
1	Graphic Power Cable, ATX 8 pin		GPU	61-140003-0H5	4
2	Terminal block 20-pin(2.54mm)		Isolated	51-2112R20-S1D	1
3	Terminal block 6-pin(10.16mm)		DC-in	51-2711R029-S1V	1
4	Terminal block 3-pin(5.0mm)		IGN/Switch	51-2411R03-S1B	1
5	P head_M2.5x6L_Ni		Mini PCIe	53-2426906-30B	2
6	P head_M3x4L_ Ni_Nylok		M.2	53-2426204-80B	7
7	H head_M4x6L_ Nylok		Wall Mount Bracket	53-M036970-216	6
8	P head_M5x10L_Ni		System on the wall	53-M023310-000	6
9	Key		SSD/HDD tray	N/A	2
10	27.8mm footpad		system	53-4029942-303	4
11	Wall Mount Bracket		system	62-03P1605-0DB	2

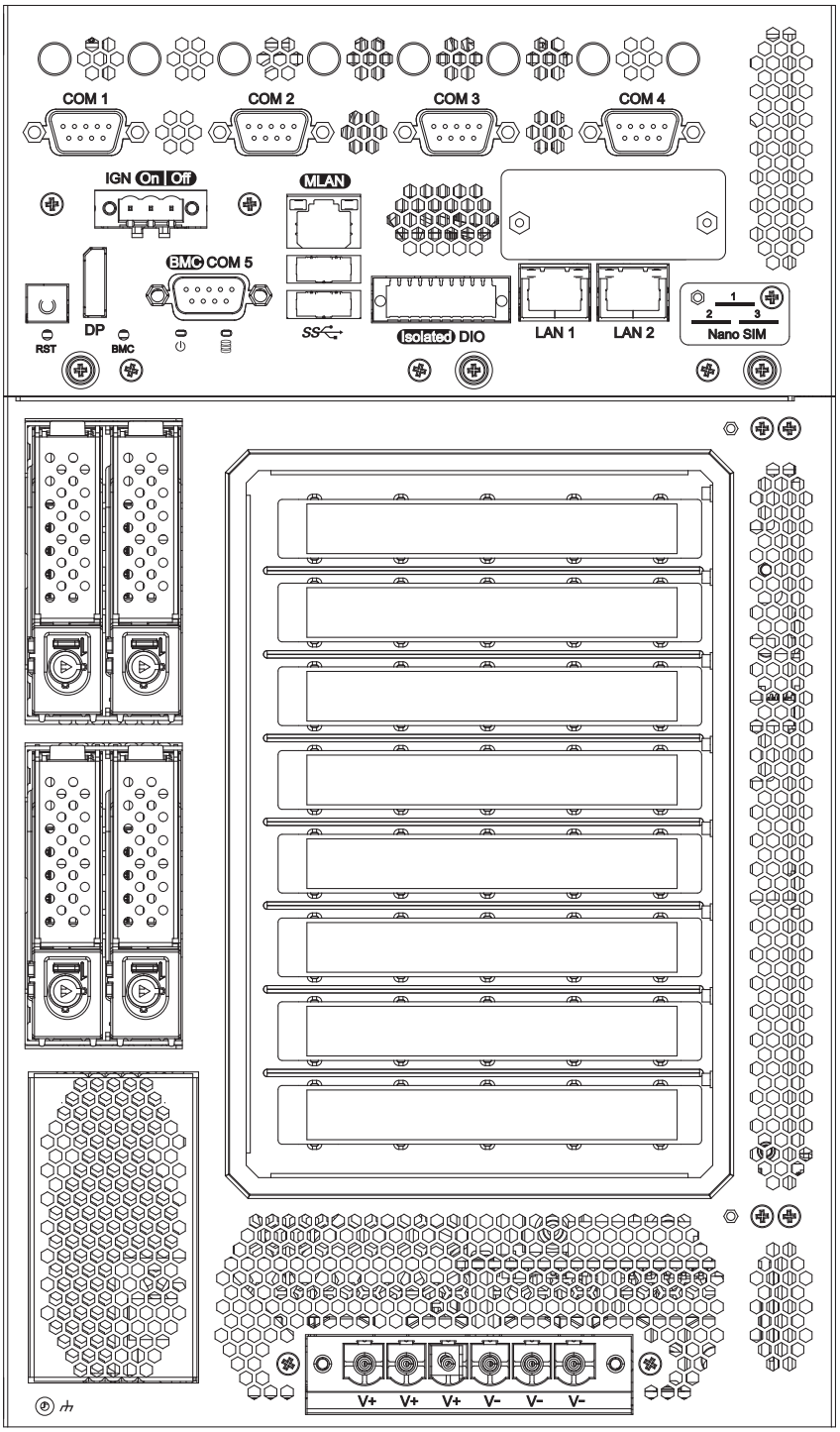
2.1.2 ICS-2000A Packing List

Item	Description	Qty
1	ICS-2000A AI Computing System (According to the configuration you order, the ICS-2000 series may contain SSD and DDR5 R DIMM. Please verify these items if necessary.)	1

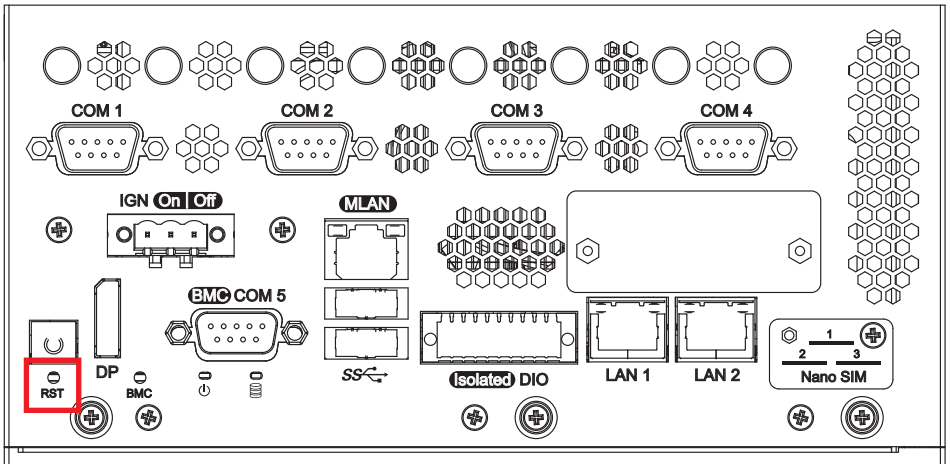
Item	Description	Outlook	Usage	P/N	Qty
1	Graphic Power Cable, ATX 8 pin		GPU	61-140003-0H5	4
2	Terminal block 20-pin(2.54mm)		Isolated	51-2112R20-S1D	1
3	Terminal block 3-pin(5.0mm)		IGN/Switch	51-2411R03-S1B	1
4	P head_M2.5x6L_Ni		Mini PCIe	53-2426906-30B	2
5	P head_M3x4L_Ni_Nylok		M.2	53-2426204-80B	7
6	H head_M4x6L_Nylok		Wall Mount Bracket	53-M036970-216	6
7	P head_M5x10L_Ni		System on the wall	53-M023310-000	6
8	Key		SSD/HDD tray	N/A	2
9	27.8mm footpad		system	53-4029942-303	4
10	Wall Mount Bracket		system	62-03P1605-0DB	2

2.2 Front Panel I/O Functions

In Vecow's ICS-2000 family, all I/O connectors are located on the front panel. Most of the general connections to the computer device, such as audio, USB, SIM, LAN, COM Port, Isolated DIO , Display Port, and any additional storage, are placed on the front panel.

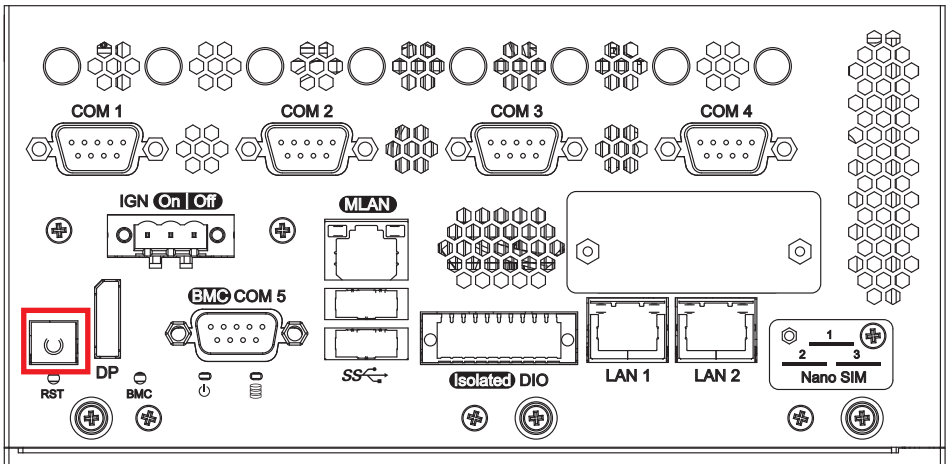


2.2.1 Reset Tact Switch



The item circled red is a hardware reset switch. Use this switch to reset the system without powering off the ICS-2000. Press and hold the reset switch for a few seconds, then reset will be enabled.

2.2.2 Power Button



The power button is a non-latched switch with dual color LED indication. It indicates power statuses: S0, S3 and S5. More details on the LED indications are listed in the following chart:

LED Color	Power Status	System Status
Solid Blue	S0	System working
Solid Orange	S3, S5	Suspend to RAM, System off with standby power

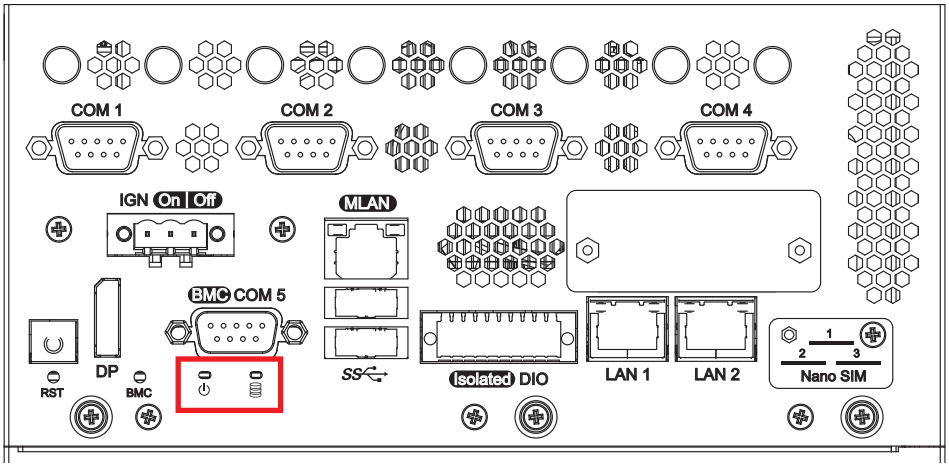
To power on ICS-2000, Either boot from G3 to S5 or G3 to S0 (by BIOS setting), you need to wait about 30 seconds for the BMC to finish booting. press the power button which will light the blue LED.

To power off ICS-2000, you can either command shutdown by OS operation or simply press the power button.

If system error appears, press and hold the power button for four seconds to shut down the machine directly.

Please do note that a four-second interval between each two power-on/power-off operation is necessary in normal working status. (For example, once turning off the system, you have to wait for four seconds to initiate another power-on operation).

2.2.3 PWR & HDD LED Indicator

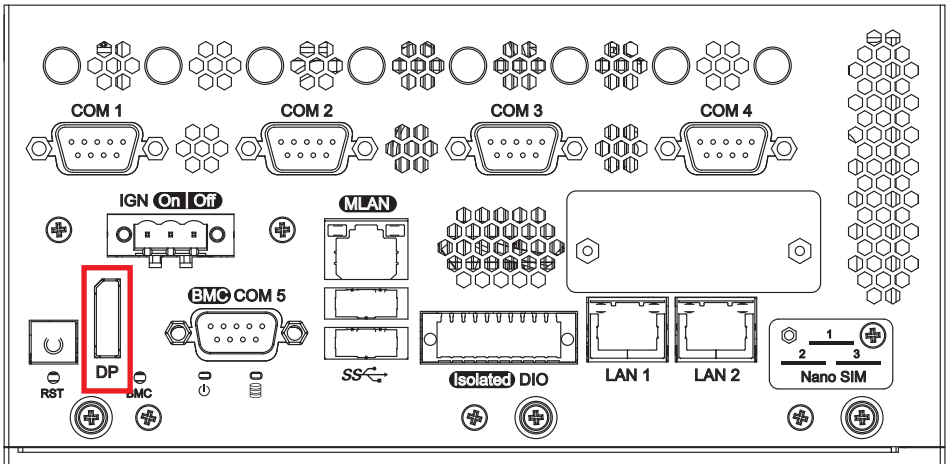


Yellow-HDD LED : A hard disk LED. If the LED is on, it indicates that the system's storage is functional. If it is off, it indicates that the system's storage is not functional. If it is flashing, it indicates data access activities are in progress.

Green-Power LED : If the LED is solid green, it indicates that the system is powered on.

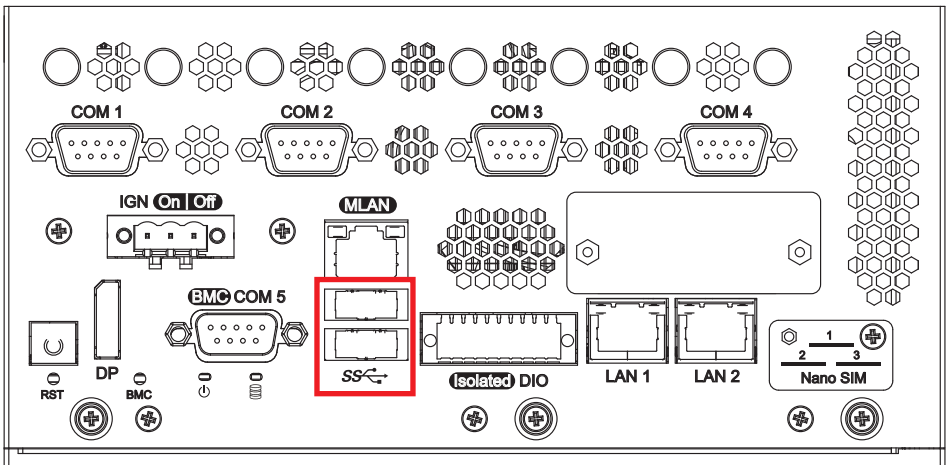
LED Color	Indication	System Status
Yellow	HDD	• On/Off : Storage status, function or not. • Twinkling : Data transferring.
Green	Power	System power status (on/off)

2.2.4 Display Port



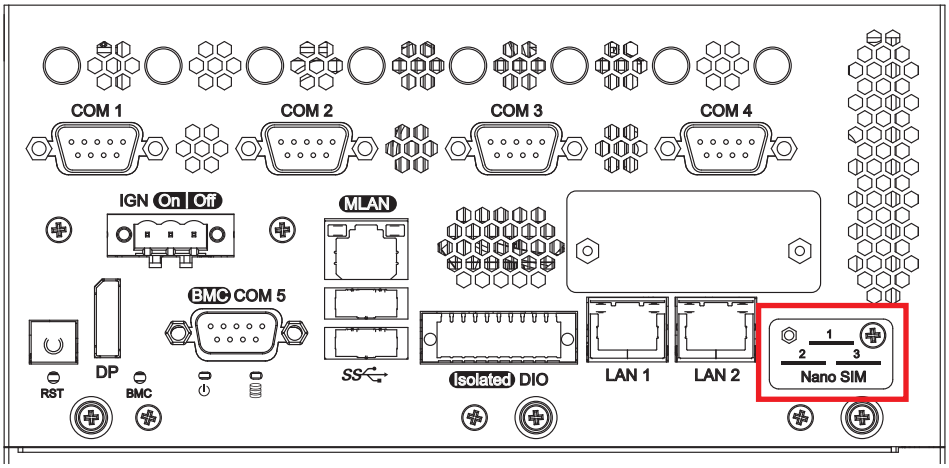
Onboard Display Port support auxiliary channel mode only , connection supports up to 1920*1080 resolution at 60 Hz.

2.2.5 USB Type-A Connector

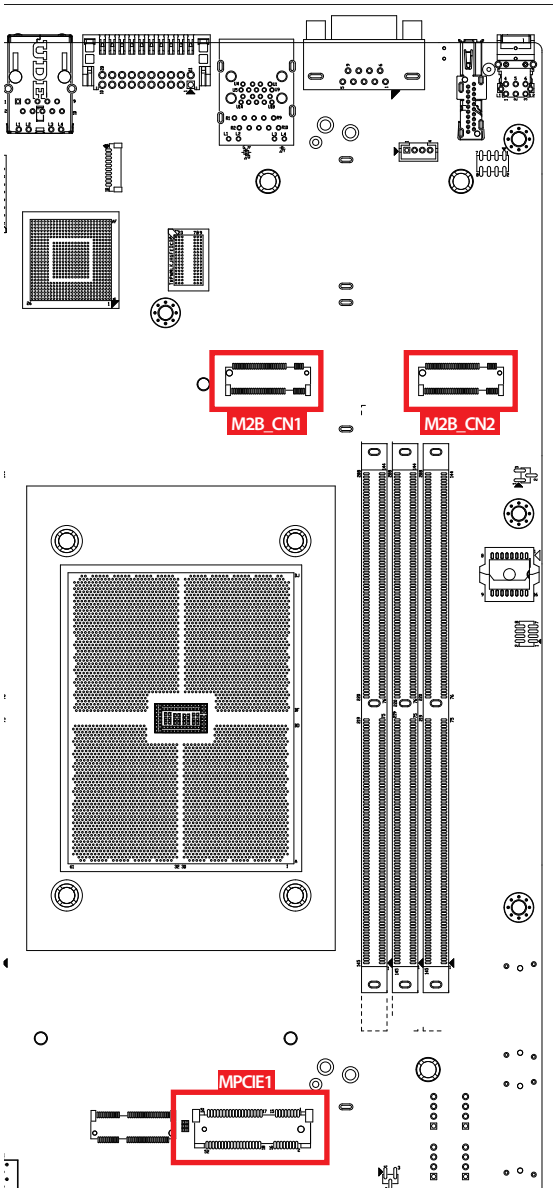


There are 2 USB 3.2 Gen1 Type A connections available supporting up to 5GB per second data rate in the front side of ICS-2000 . It also compliant with the requirements of Super Speed (SS), high speed (HS), full speed (FS) and low speed (LS).

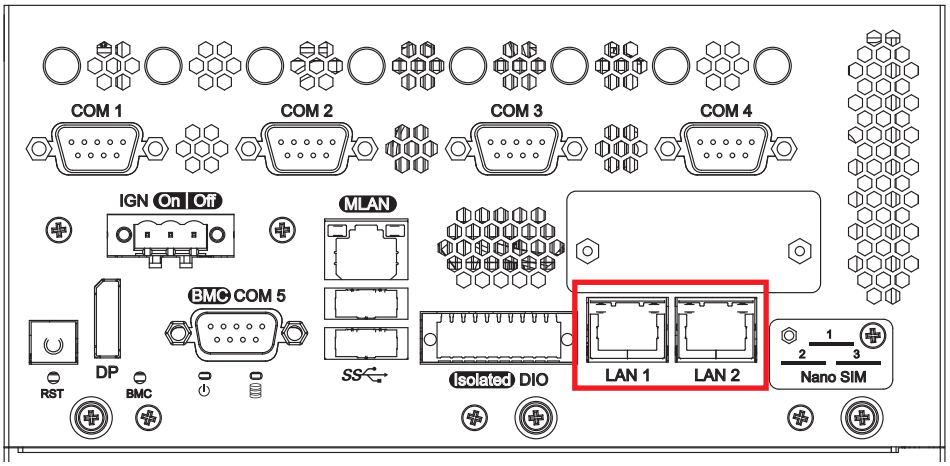
2.2.6 Nano SIM 1, Nano SIM 2 , Nano SIM 3



Slot	SIM
MPCIE	Nano SIM1
M2B_CN2	Nano SIM2
M2B_CN1	Nano SIM3



2.2.7 10/100/1000 Mbps Ethernet Port

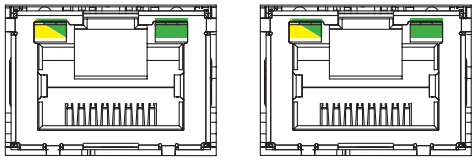


There are two 8-pin RJ-45 jacks supporting 10/100/1000 Mbps Ethernet connections on the front side of ICS-2000. LAN1, LAN 2 is powered by Intel I350 Ethernet engine.

Using suitable RJ-45 cable, you can connect the ICS-2000 system to a computer or to any other devices with Ethernet connection, for example, a hub or a switch. Moreover, LAN 1 and LAN 2 support “Wake” on LAN functions. The pinouts are listed in the following chart:

Pin Number	10/100 Mbps	1000Mbps
1	E_TX+	MDI0_P
2	E_TX-	MDI0_N
3	E_RX+	MDI1_P
4	----	MDI2_P
5	-----	MDI2_N
6	E_RX-	MDI1_N
7	-----	MDI3_P
8	------	MDI3_N

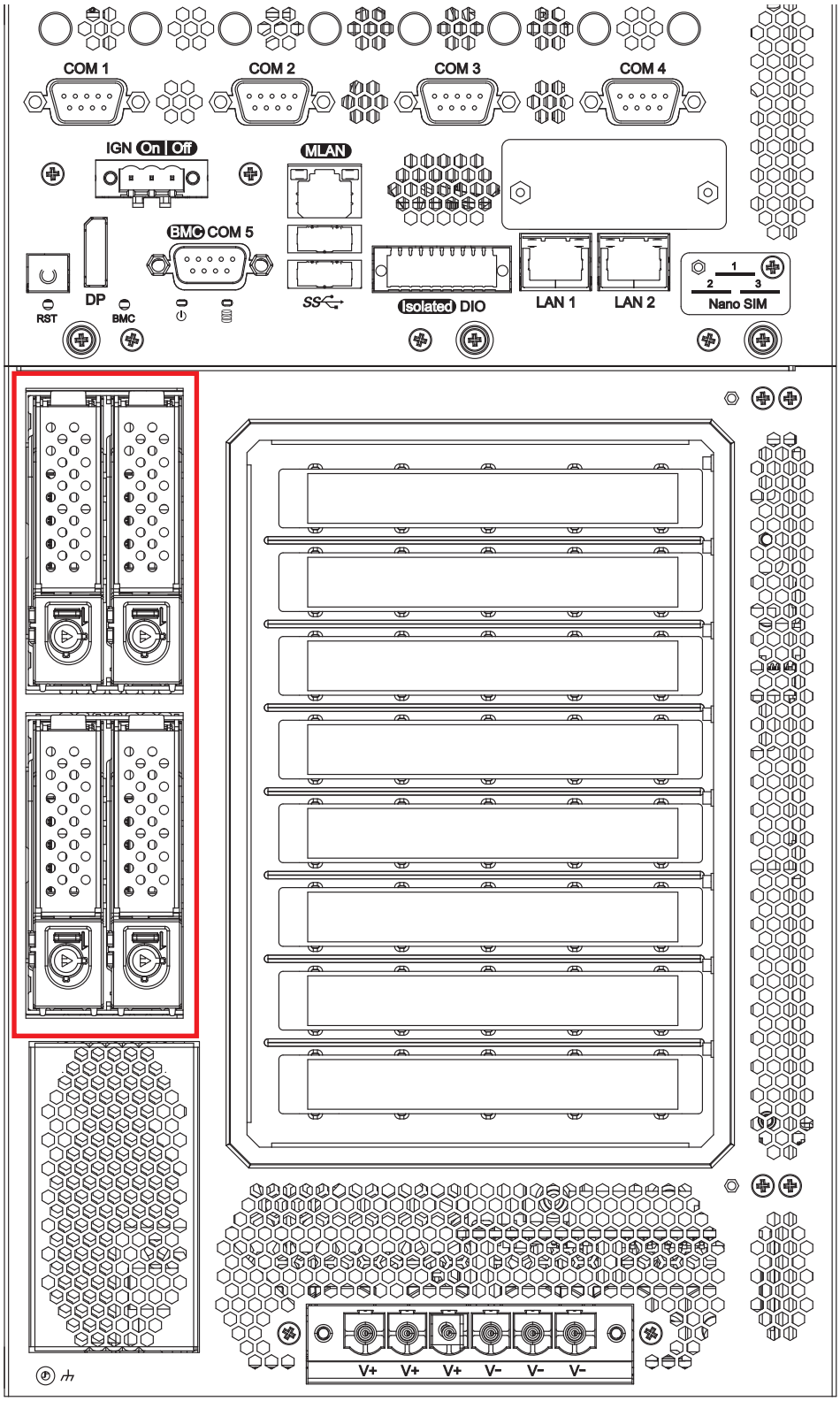
Each LAN port is supported by a standard RJ-45 connector with LED indicators to present active/link/speed statuses of the connection.



LAN1 LAN2

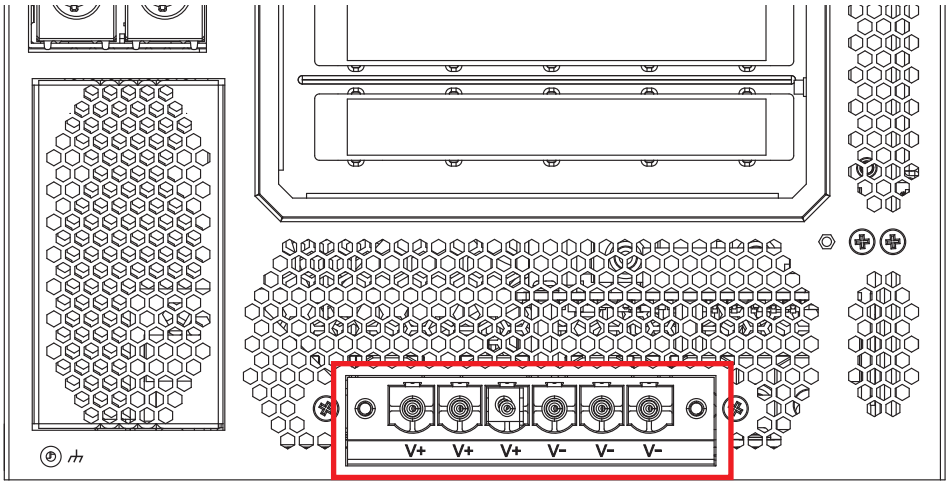
LED Location	LED Color	10Mbps	100Mbps	1000 Mbps
Right	Yellow	Twinkling Yellow	Twinkling Yellow	Twinkling Yellow
Left	Green/Yellow	Off	Green	Yellow

2.2.8 Front-access U.2 Tray



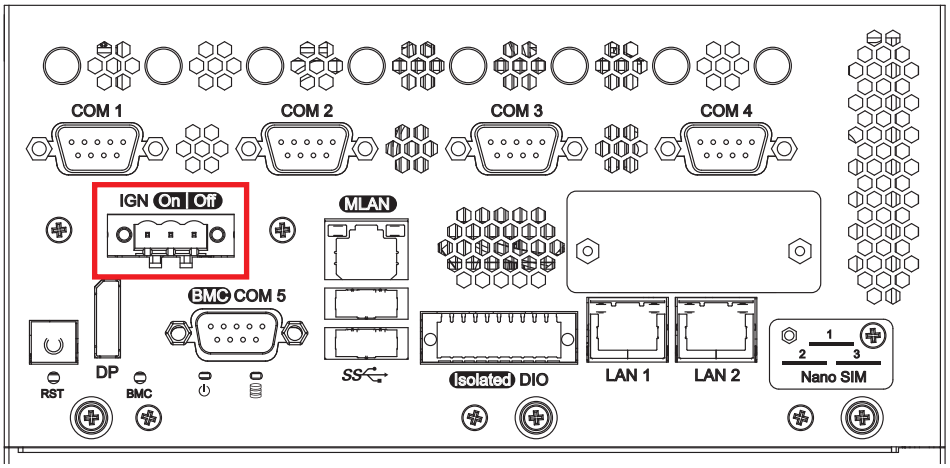
There are four front-access 2.5” U.2 trays on the front side of ICS-2000. Press the trigger to open the U.2 tray which has up to 8TB available.

2.2.9 Power Terminal Block

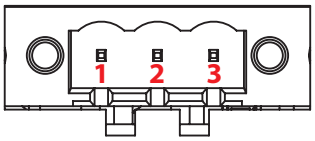


ICS-2000 supports 16V to 50V DC power input.

2.2.10 Remote Power On/Off Switch & IGN ITION Terminal Block

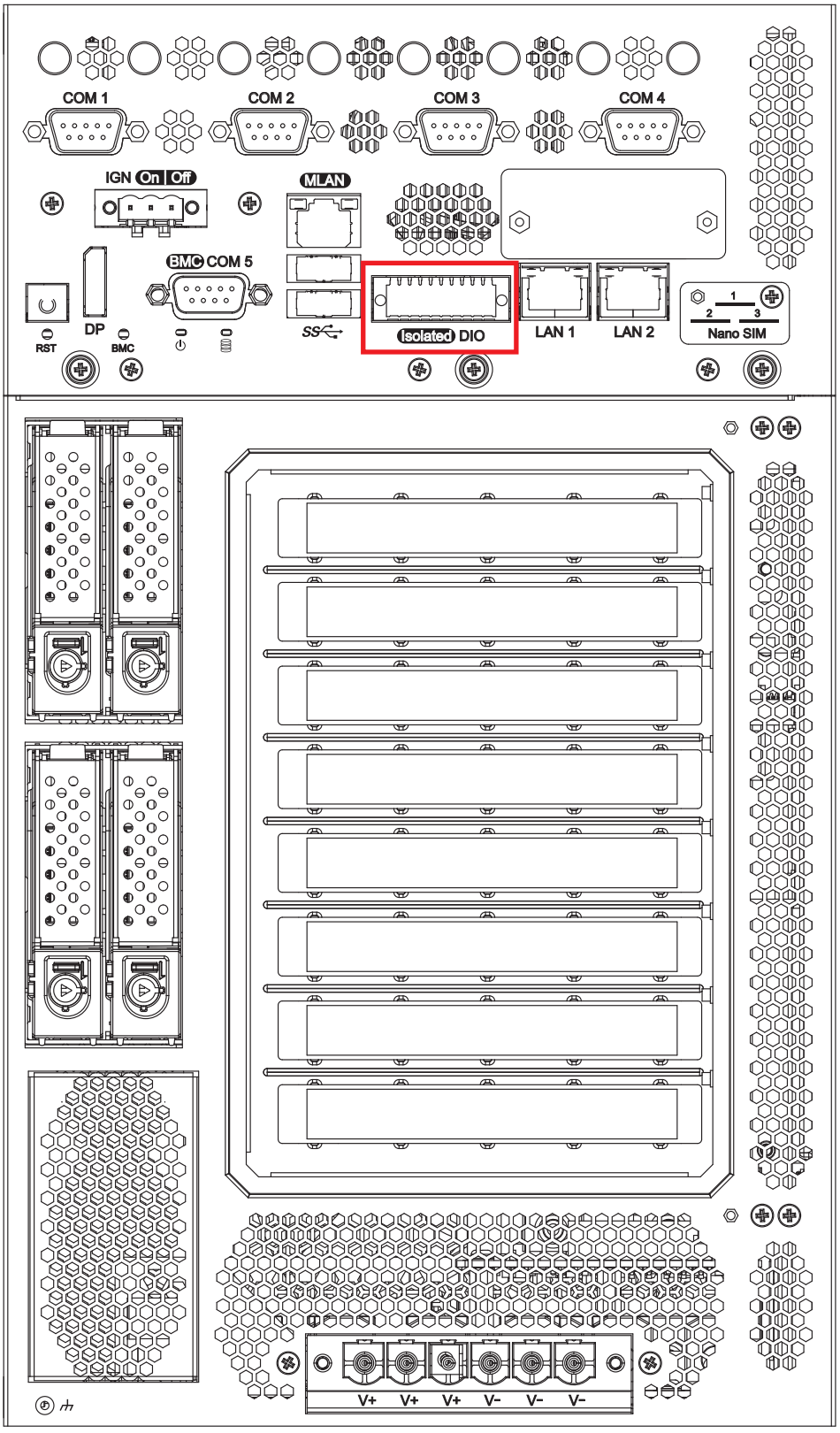


It is a 2-pin power-on/power-off switch through Phoenix Contact terminal block. You could turn on or off the system power by using this contact. This terminal block supports dual function on soft power-on/ power-off (instant off or delay four seconds), and suspend mode.



Pin No.	Definition
1	IGNITION
2	SW+
3	SW-

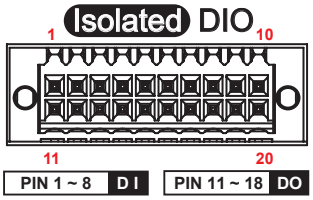
2.2.11 Isolated DIO



There is a 16-bit (8-bit DI, 8-bit DO) connectors in the front side. DI/DIO support NPN (sink) and PNP (Source) mode, Each DI channel is equipped with a photocouper for isolated protection. Each DO with isolator chip, Config by a Jumper for each DIO connector.

DO Safety-Related Certifications :

- 4242-VPK Basic Isolation per DIN V VDE V 0884-10 and DIN EN 61010-1
- 3-KVRMS Isolation for 1 minute per UL 1577
- CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
- GB4943.1-2011 CQC Certified

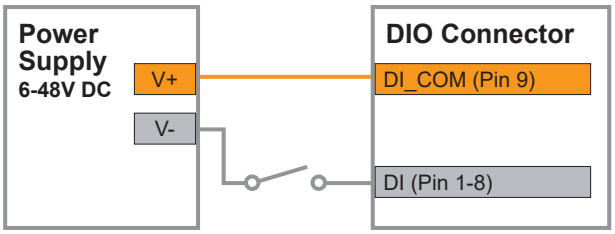


DIO1 Connectors pin out :

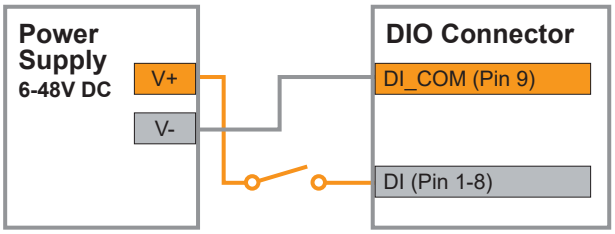
Pin No.	Definition	Mapping to SIO GPIO Function
1	INPUT 0	SIO_GPI80
2	INPUT 1	SIO_GPI81
3	INPUT 2	SIO_GPI82
4	INPUT 3	SIO_GPI83
5	INPUT 4	SIO_GPI84
6	INPUT 5	SIO_GPI85
7	INPUT 6	SIO_GPI86
8	INPUT 7	SIO_GPI87
9	+VDI_COM1	
10	GND_ISO_DIO1	
11	OUTPUT 0	SIO_GPO70
12	OUTPUT 1	SIO_GPO71
13	OUTPUT 2	SIO_GPO72
14	OUTPUT 3	SIO_GPO73
15	OUTPUT 4	SIO_GPO74
16	OUTPUT 5	SIO_GPO75
17	OUTPUT 6	SIO_GPO76
18	OUTPUT 7	SIO_GPO77
19	GND_ISO_DIO1	
20	External 6-40VDC (NPN) External 6-48VDC (PNP)	

DI reference circuit :

Sink Mode (NPN)

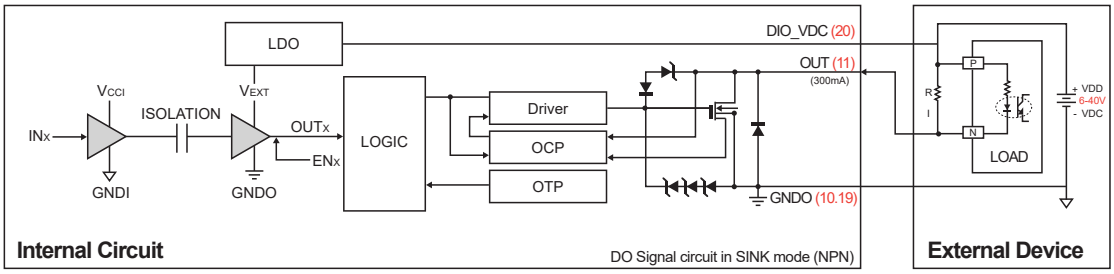


Source Mode (PNP)

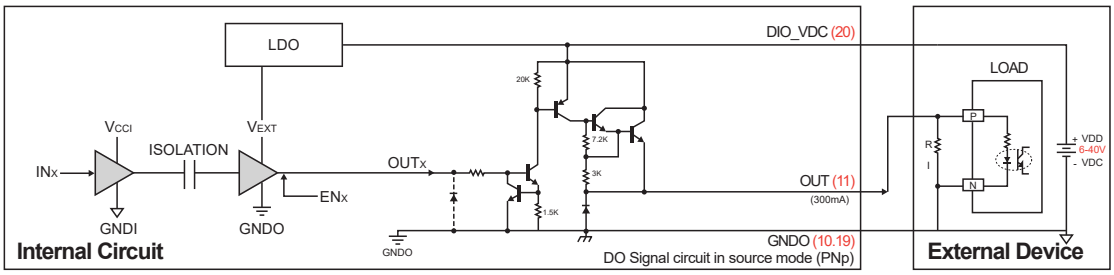


DO reference circuit :

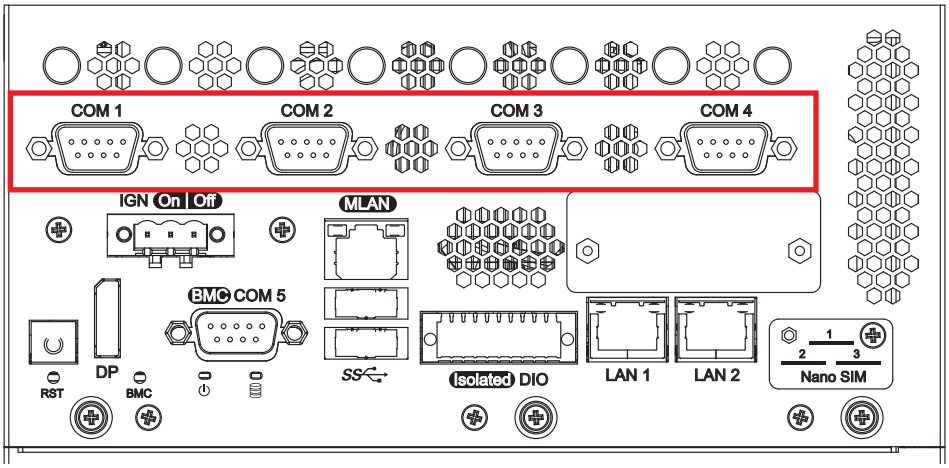
Sink Mode (NPN, Default)



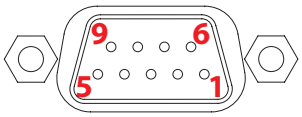
Source (PNP)



2.2.12 Serial Port COM



Serial port can be configured for RS-232, RS-422, or RS-485 with auto flow control communication. The default definition is RS-232, but if you want to change to RS-422 or RS-485, you can find the settings in BIOS.

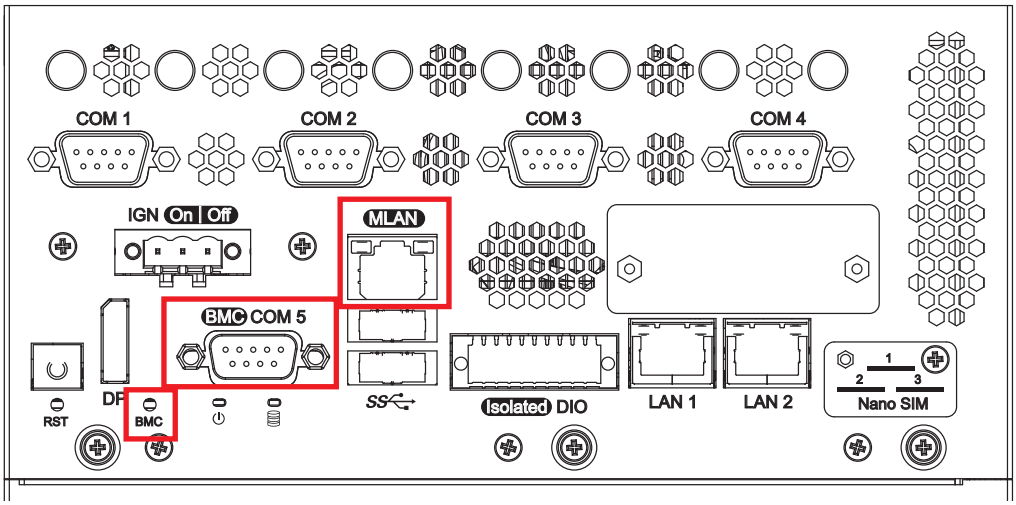


BIOS Setting	Function
COM 1 COM 2 COM 3 COM 4	RS-232
	RS-422 (5-wire)
	RS-485
	RS-485 w/z auto-flow control

The pin assignments are listed in the table as follows :

Serial Port	Pin No.	RS-232	RS-422 (5-wire)	RS-485 (3-wire)
1, 2 3, 4	1	DCD	TXD-	DATA-
	2	RXD	TXD+	DATA+
	3	TXD	RXD+	----------
	4	DTR	RXD-	----------
	5	GND	GND	GND
	6	DSR	----------	----------
	7	RTS	----------	----------
	8	CTS	----------	----------
	9	RI	----------	----------

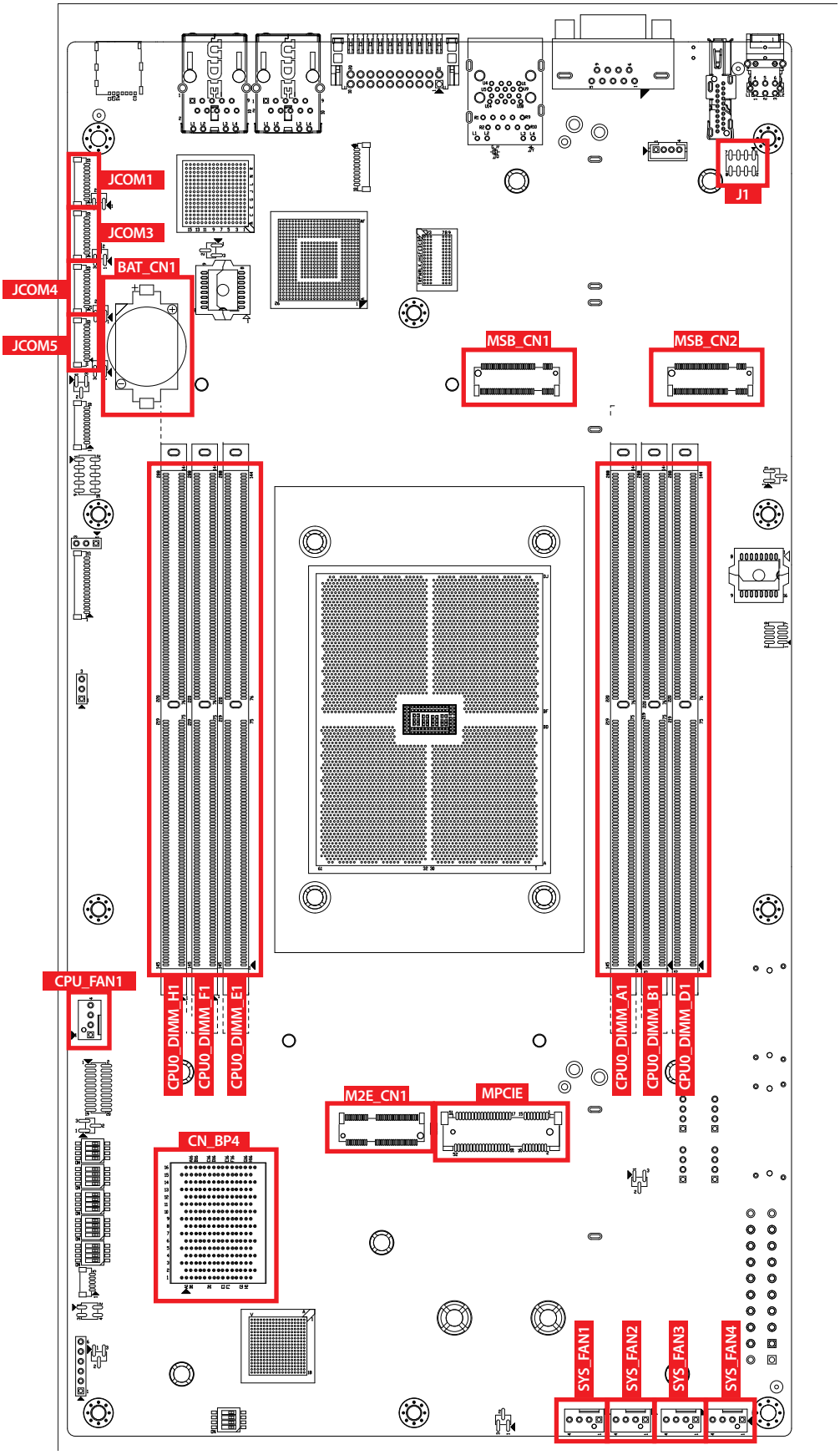
2.2.13 BMC bottom ,MLAN and COM5



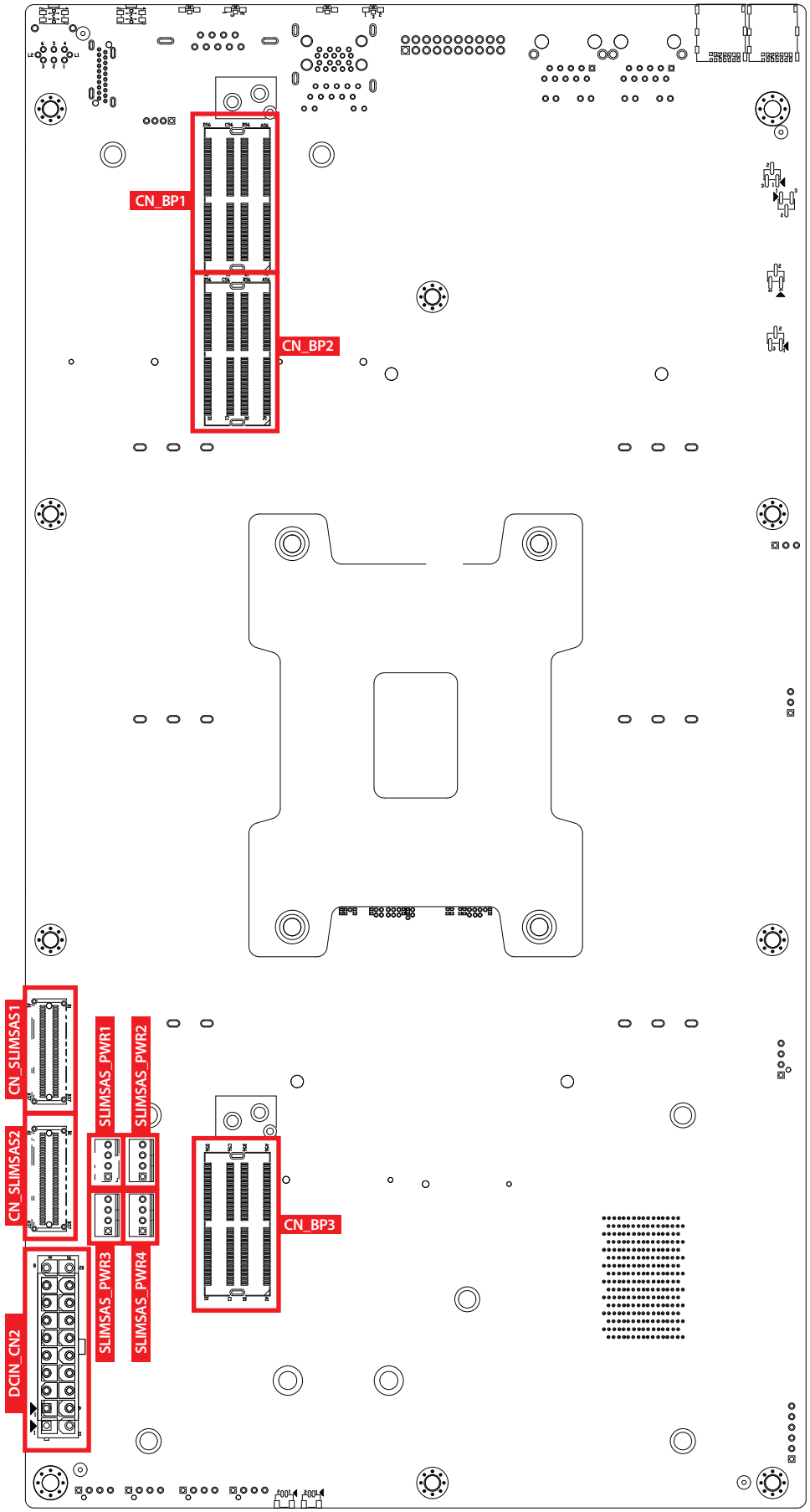
BMC bottom, MLAN and COM5 is used for BMC function use only.

2.3 Main Board Expansion Connectors

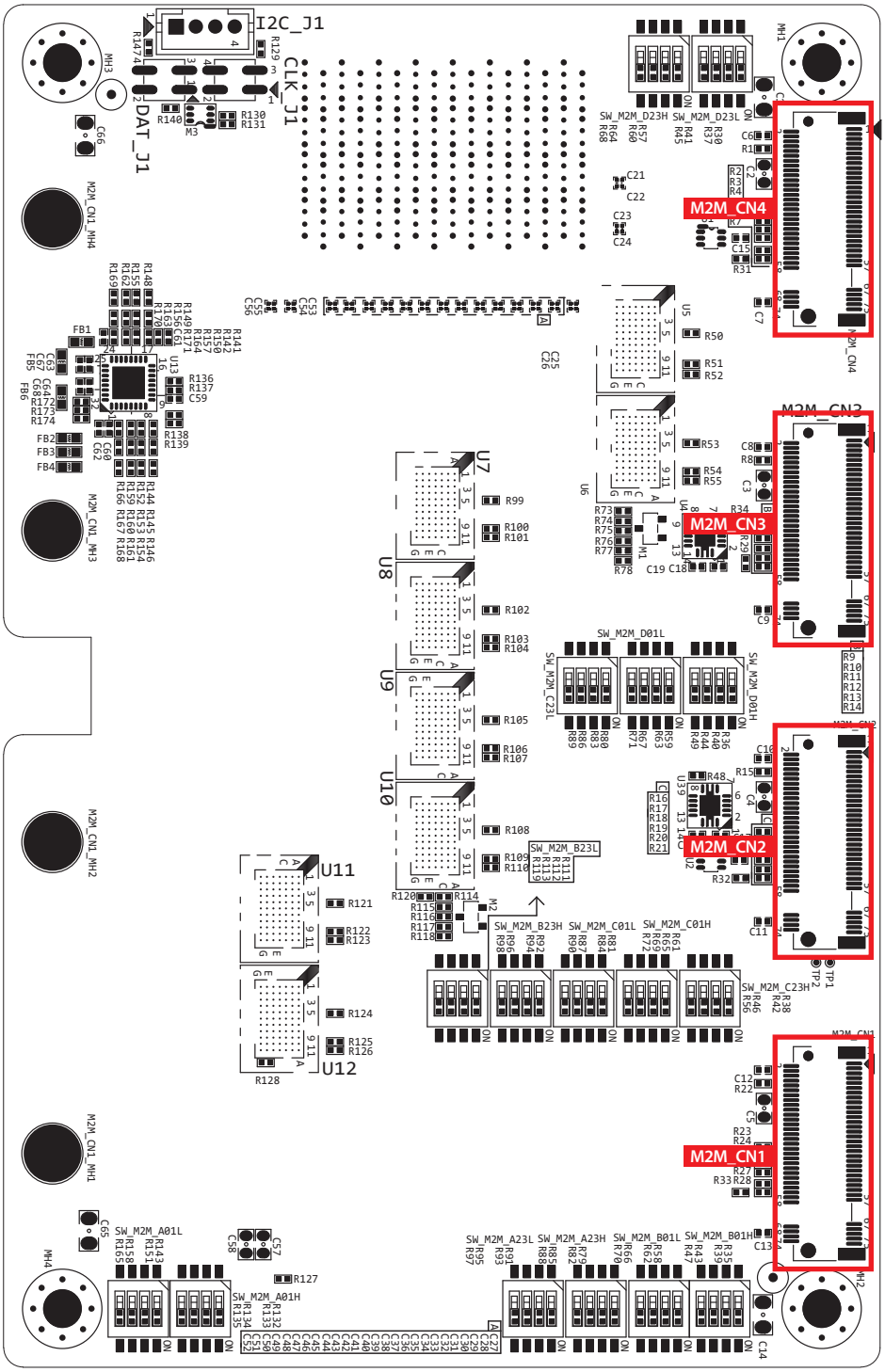
2.3.1 Front View of ICS-2000 Main Board With Connector Location



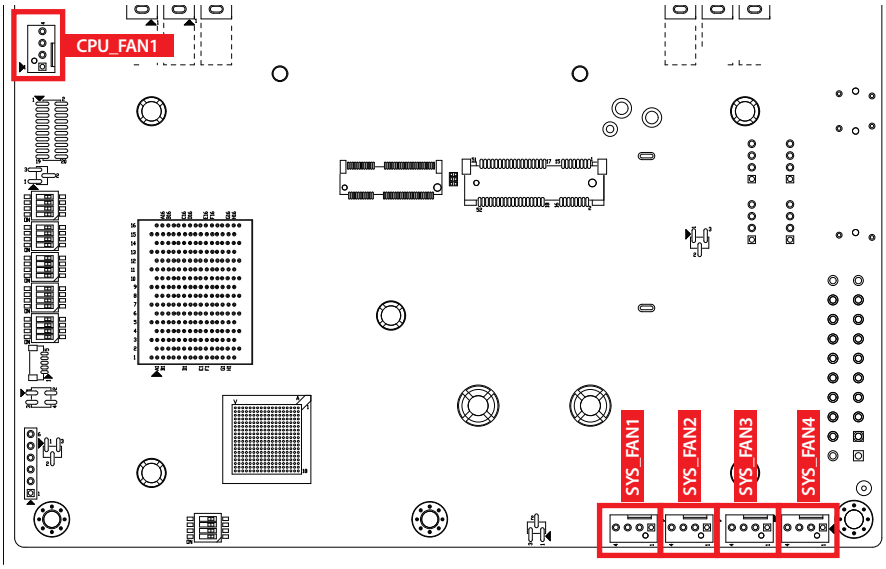
2.3.2 Rear View of ICS-2000 Main Board With Connector Location



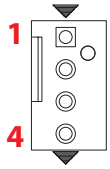
2.3.3 View of ICS-2000 M2D Board With Connector Location



2.3.4 CPU_FAN, SYS_FAN1, SYS_FAN2, SYS_FAN3, SYS_FAN4

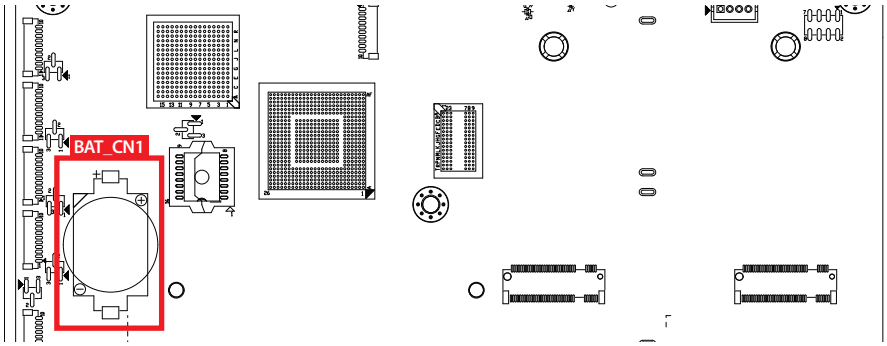


The fan power connector is for additional thermal requirements. The pin assignments of CPU_FAN, SYS_FAN1, SYS_FAN2, SYS_FAN3, SYS_FAN4 are listed in the following table:



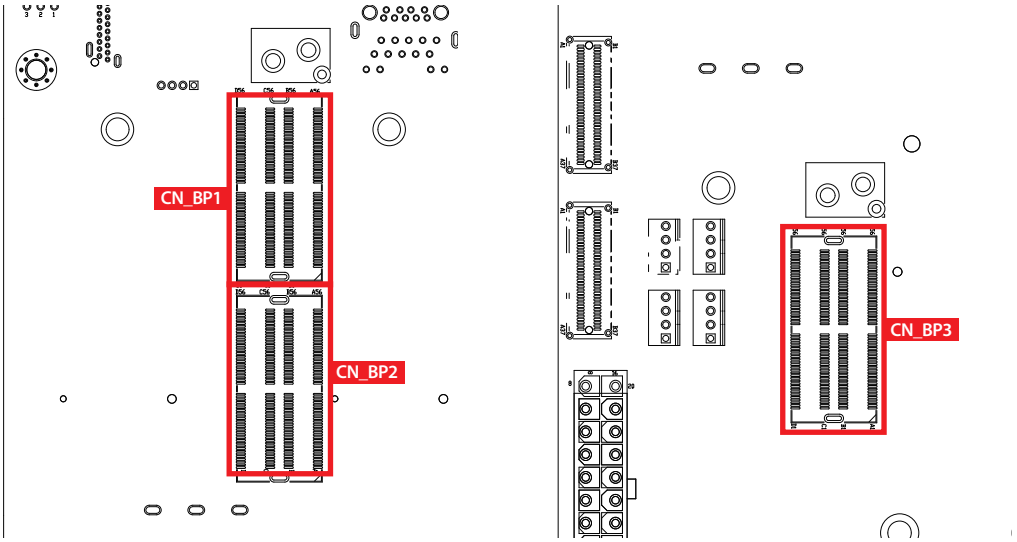
CPU_FAN, SYS_FAN1, SYS_FAN2, SYS_FAN3, SYS_FAN4	
Pin No.	Description
1	GND
2	+12V (up to 2A)
3	Fan speed sensor
4	Fan PWM

2.3.5 BAT_CN1 : Battery

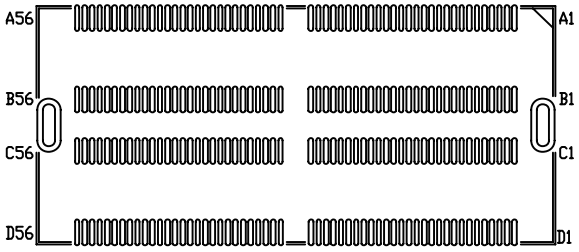


The ICS-2000's real-time clock is powered by a lithium battery. It is equipped with Panasonic CR2032 220mAh lithium battery. It is recommended that you do not replace the lithium battery on your own. If the battery needs to be changed, please contact the Vecow RMA service team.

2.3.6 CN_BP1~3 : Board to Board Conn



The pin assignments of CN_BP1~3 are listed in the following table :



Pin No.	Function	Pin No.	Function
CN_BP1			
A1	GND	B1	GND
A2	PCIE_x16_slot_A7_TX_P	B2	PCIE_x16_slot_B7_TX_P
A3	PCIE_x16_slot_A7_TX_N	B3	PCIE_x16_slot_B7_TX_N
A4	GND	B4	GND
A5	PCIE_x16_slot_A6_TX_P	B5	PCIE_x16_slot_B6_TX_P
A6	PCIE_x16_slot_A6_TX_N	B6	PCIE_x16_slot_B6_TX_N
A7	GND	B7	GND
A8	PCIE_x16_slot_A5_TX_P	B8	PCIE_x16_slot_B5_TX_P
A9	PCIE_x16_slot_A5_TX_N	B9	PCIE_x16_slot_B5_TX_N
A10	GND	B10	GND
A11	PCIE_x16_slot_A4_TX_P	B11	PCIE_x16_slot_B4_TX_P
A12	PCIE_x16_slot_A4_TX_N	B12	PCIE_x16_slot_B4_TX_N
A13	GND	B13	GND
A14	PCIE_x16_slot_A3_TX_P	B14	PCIE_x16_slot_B3_TX_P
A15	PCIE_x16_slot_A3_TX_N	B15	PCIE_x16_slot_B3_TX_N
A16	GND	B16	GND
A17	PCIE_x16_slot_A2_TX_P	B17	PCIE_x16_slot_B2_TX_P

A18	PCIE_x16_slot_A2_TX_N	B18	PCIE_x16_slot_B2_TX_N
A19	GND	B19	GND
A20	PCIE_x16_slot_A1_TX_P	B20	PCIE_x16_slot_B1_TX_P
A21	PCIE_x16_slot_A1_TX_N	B21	PCIE_x16_slot_B1_TX_N
A22	GND	B22	GND
A23	PCIE_x16_slot_A0_TX_P	B23	PCIE_x16_slot_B0_TX_P
A24	PCIE_x16_slot_A0_TX_N	B24	PCIE_x16_slot_B0_TX_N
A25	GND	B25	GND
A26	NC	B26	NC
A27	NC	B27	NC
A28	NC	B28	NC
A29	GND	B29	GND
A30	PCIE_x16_slot_A7_RX_P	B30	PCIE_x16_slot_B7_RX_P
A31	PCIE_x16_slot_A7_RX_N	B31	PCIE_x16_slot_B7_RX_N
A32	GND	B32	GND
A33	PCIE_x16_slot_A6_RX_P	B33	PCIE_x16_slot_B6_RX_P
A34	PCIE_x16_slot_A6_RX_N	B34	PCIE_x16_slot_B6_RX_N
A35	GND	B35	GND
A36	PCIE_x16_slot_A5_RX_P	B36	PCIE_x16_slot_B5_RX_P
A37	PCIE_x16_slot_A5_RX_N	B37	PCIE_x16_slot_B5_RX_N
A38	GND	B38	GND
A39	PCIE_x16_slot_A4_RX_P	B39	PCIE_x16_slot_B4_RX_P
A40	PCIE_x16_slot_A4_RX_N	B40	PCIE_x16_slot_B4_RX_N
A41	GND	B41	GND
A42	PCIE_x16_slot_A3_RX_P	B42	PCIE_x16_slot_B3_RX_P
A43	PCIE_x16_slot_A3_RX_N	B43	PCIE_x16_slot_B3_RX_N
A44	GND	B44	GND
A45	PCIE_x16_slot_A2_RX_P	B45	PCIE_x16_slot_B2_RX_P
A46	PCIE_x16_slot_A2_RX_N	B46	PCIE_x16_slot_B2_RX_N
A47	GND	B47	GND
A48	PCIE_x16_slot_A1_RX_P	B48	PCIE_x16_slot_B1_RX_P
A49	PCIE_x16_slot_A1_RX_N	B49	PCIE_x16_slot_B1_RX_N
A50	GND	B50	GND
A51	PCIE_x16_slot_A0_RX_P	B51	PCIE_x16_slot_B0_RX_P
A52	PCIE_x16_slot_A0_RX_N	B52	PCIE_x16_slot_B0_RX_N
A53	GND	B53	GND
A54	SMB_PCH_SMBDATA	B54	P12V_BP_SDA
A55	SMB_PCH_SMBCLK	B55	P12V_BP_SCL
A56	GND	B56	GND
C1	GND	D1	GND
C2	PCIE_x8_slot_A7_TX_P	D2	GND
C3	PCIE_x8_slot_A7_TX_N	D3	GND

C4	GND	D4	GND
C5	PCIE_x8_slot_A6_TX_P	D5	GND
C6	PCIE_x8_slot_A6_TX_N	D6	GND
C7	GND	D7	GND
C8	PCIE_x8_slot_A5_TX_P	D8	GND
C9	PCIE_x8_slot_A5_TX_N	D9	GND
C10	GND	D10	GND
C11	PCIE_x8_slot_A4_TX_P	D11	GND
C12	PCIE_x8_slot_A4_TX_N	D12	GND
C13	GND	D13	GND
C14	PCIE_x8_slot_A3_TX_P	D14	GND
C15	PCIE_x8_slot_A3_TX_N	D15	GND
C16	GND	D16	GND
C17	PCIE_x8_slot_A2_TX_P	D17	GND
C18	PCIE_x8_slot_A2_TX_N	D18	GND
C19	GND	D19	GND
C20	PCIE_x8_slot_A1_TX_P	D20	GND
C21	PCIE_x8_slot_A1_TX_N	D21	GND
C22	GND	D22	GND
C23	PCIE_x8_slot_A0_TX_P	D23	GND
C24	PCIE_x8_slot_A0_TX_N	D24	GND
C25	GND	D25	GND
C26	BMC_PWM6_BP	D26	GND
C27	FANTACH6	D27	GND
C28	GND	D28	GND
C29	GND	D29	GND
C30	PCIE_x8_slot_A7_RX_P	D30	GND
C31	PCIE_x8_slot_A7_RX_N	D31	PCIE_x16_slot_A_PRSNT
C32	GND	D32	GND
C33	PCIE_x8_slot_A6_RX_P	D33	PCIE_x16_slot_B_PRSNT
C34	PCIE_x8_slot_A6_RX_N	D34	GND
C35	GND	D35	GND
C36	PCIE_x8_slot_A5_RX_P	D36	GND
C37	PCIE_x8_slot_A5_RX_N	D37	GND
C38	GND	D38	GND
C39	PCIE_x8_slot_A4_RX_P	D39	PCIE_x8_slot_A_PRSNT
C40	PCIE_x8_slot_A4_RX_N	D40	GND
C41	GND	D41	PCIE_x8_slot_B_PRSNT
C42	PCIE_x8_slot_A3_RX_P	D42	GND
C43	PCIE_x8_slot_A3_RX_N	D43	PCIE_x8_slot_C_PRSNT
C44	GND	D44	GND
C45	PCIE_x8_slot_A2_RX_P	D45	PCIE_x8_slot_D_PRSNT

C46	PCIE_x8_slot_A2_RX_N	D46	GND
C47	GND	D47	P12V_BP1_ALERT_N
C48	PCIE_x8_slot_A1_RX_P	D48	GND
C49	PCIE_x8_slot_A1_RX_N	D49	P12V_BP2_ALERT_N
C50	GND	D50	GND
C51	PCIE_x8_slot_A0_RX_P	D51	GND
C52	PCIE_x8_slot_A0_RX_N	D52	GND
C53	GND	D53	GND
C54	BMC_PWM7_BP	D54	GND
C55	FANTACH7	D55	GND
C56	GND	D56	GND
CN_BP2			
A1	GND	B1	GND
A2	PCIE_x16_slot_A15_RX_P	B2	PCIE_x16_slot_B15_RX_P
A3	PCIE_x16_slot_A15_RX_N	B3	PCIE_x16_slot_B15_RX_N
A4	GND	B4	GND
A5	PCIE_x16_slot_A14_RX_P	B5	PCIE_x16_slot_B14_RX_P
A6	PCIE_x16_slot_A14_RX_N	B6	PCIE_x16_slot_B14_RX_N
A7	GND	B7	GND
A8	PCIE_x16_slot_A13_RX_P	B8	PCIE_x16_slot_B13_RX_P
A9	PCIE_x16_slot_A13_RX_N	B9	PCIE_x16_slot_B13_RX_N
A10	GND	B10	GND
A11	PCIE_x16_slot_A12_RX_P	B11	PCIE_x16_slot_B12_RX_P
A12	PCIE_x16_slot_A12_RX_N	B12	PCIE_x16_slot_B12_RX_N
A13	GND	B13	GND
A14	PCIE_x16_slot_A11_RX_P	B14	PCIE_x16_slot_B11_RX_P
A15	PCIE_x16_slot_A11_RX_N	B15	PCIE_x16_slot_B11_RX_N
A16	GND	B16	GND
A17	PCIE_x16_slot_A10_RX_P	B17	PCIE_x16_slot_B10_RX_P
A18	PCIE_x16_slot_A10_RX_N	B18	PCIE_x16_slot_B10_RX_N
A19	GND	B19	GND
A20	PCIE_x16_slot_A9_RX_P	B20	PCIE_x16_slot_B9_RX_P
A21	PCIE_x16_slot_A9_RX_N	B21	PCIE_x16_slot_B9_RX_N
A22	GND	B22	GND
A23	PCIE_x16_slot_A8_RX_P	B23	PCIE_x16_slot_B8_RX_P
A24	PCIE_x16_slot_A8_RX_N	B24	PCIE_x16_slot_B8_RX_N
A25	GND	B25	GND
A26	BMC_SMB_PCIEX16_A_SDA	B26	BMC_SMB_PCIEX16_B_SDA
A27	BMC_SMB_PCIEX16_A_SCL	B27	BMC_SMB_PCIEX16_B_SCL
A28	GND	B28	GND
A29	GND	B29	GND
A30	PCIE_x16_slot_A15_RX_P	B30	PCIE_x16_slot_B15_RX_P

A31	PCIE_x16_slot_A15_RX_N	B31	PCIE_x16_slot_B15_RX_N
A32	GND	B32	GND
A33	PCIE_x16_slot_A14_RX_P	B33	PCIE_x16_slot_B14_RX_P
A34	PCIE_x16_slot_A14_RX_N	B34	PCIE_x16_slot_B14_RX_N
A35	GND	B35	GND
A36	PCIE_x16_slot_A13_RX_P	B36	PCIE_x16_slot_B13_RX_P
A37	PCIE_x16_slot_A13_RX_N	B37	PCIE_x16_slot_B13_RX_N
A38	GND	B38	GND
A39	PCIE_x16_slot_A12_RX_P	B39	PCIE_x16_slot_B12_RX_P
A40	PCIE_x16_slot_A12_RX_N	B40	PCIE_x16_slot_B12_RX_N
A41	GND	B41	GND
A42	PCIE_x16_slot_A11_RX_P	B42	PCIE_x16_slot_B11_RX_P
A43	PCIE_x16_slot_A11_RX_N	B43	PCIE_x16_slot_B11_RX_N
A44	GND	B44	GND
A45	PCIE_x16_slot_A10_RX_P	B45	PCIE_x16_slot_B10_RX_P
A46	PCIE_x16_slot_A10_RX_N	B46	PCIE_x16_slot_B10_RX_N
A47	GND	B47	GND
A48	PCIE_x16_slot_A9_RX_P	B48	PCIE_x16_slot_B9_RX_P
A49	PCIE_x16_slot_A9_RX_N	B49	PCIE_x16_slot_B9_RX_N
A50	GND	B50	GND
A51	PCIE_x16_slot_A8_RX_P	B51	PCIE_x16_slot_B8_RX_P
A52	PCIE_x16_slot_A8_RX_N	B52	PCIE_x16_slot_B8_RX_N
A53	GND	B53	GND
A54	BMC_SMB_PCIEX8_D_SDA	B54	BMC_SMB_PCIEX8_C_SDA
A55	BMC_SMB_PCIEX8_D_SCL	B55	BMC_SMB_PCIEX8_C_SCL
A56	GND	B56	GND
C1	GND	D1	NC
C2	PCIE_x8_slot_B7_RX_P	D2	GND
C3	PCIE_x8_slot_B7_RX_N	D3	GND
C4	GND	D4	GND
C5	PCIE_x8_slot_B6_RX_P	D5	GND
C6	PCIE_x8_slot_B6_RX_N	D6	GND
C7	GND	D7	GND
C8	PCIE_x8_slot_B5_RX_P	D8	GND
C9	PCIE_x8_slot_B5_RX_N	D9	GND
C10	GND	D10	GND
C11	PCIE_x8_slot_B4_RX_P	D11	GND
C12	PCIE_x8_slot_B4_RX_N	D12	GND
C13	GND	D13	GND
C14	PCIE_x8_slot_B3_RX_P	D14	GND

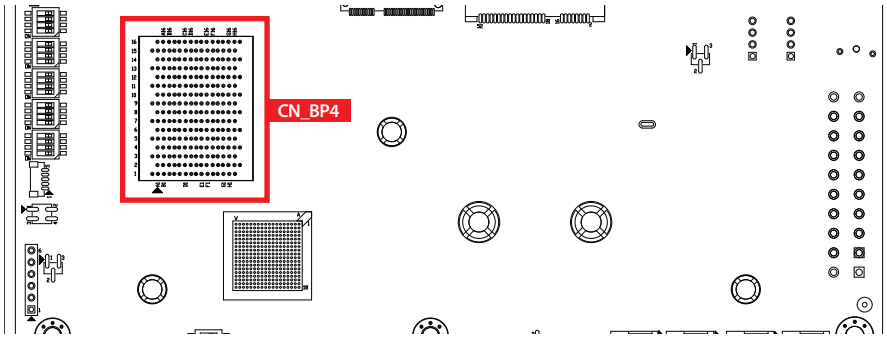
C15	PCIE_x8_slot_B3_RX_N	D15	GND
C16	GND	D16	GND
C17	PCIE_x8_slot_B2_RX_P	D17	GND
C18	PCIE_x8_slot_B2_RX_N	D18	GND
C19	GND	D19	GND
C20	PCIE_x8_slot_B1_RX_P	D20	GND
C21	PCIE_x8_slot_B1_RX_N	D21	GND
C22	GND	D22	GND
C23	PCIE_x8_slot_B0_RX_P	D23	GND
C24	PCIE_x8_slot_B0_RX_N	D24	GND
C25	GND	D25	GND
C26	BMC_SMB_PCIEX8_A_SDA	D26	GND
C27	BMC_SMB_PCIEx8_A_SCL	D27	GND
C28	GND	D28	GND
C29	GND	D29	GND
C30	PCIE_x8_slot_B7_RX_P	D30	PCIEx16_A_RST
C31	PCIE_x8_slot_B7_RX_N	D31	GND
C32	GND	D32	PCIEx16_B_RST
C33	PCIE_x8_slot_B6_RX_P	D33	GND
C34	PCIE_x8_slot_B6_RX_N	D34	GND
C35	GND	D35	GND
C36	PCIE_x8_slot_B5_RX_P	D36	GND
C37	PCIE_x8_slot_B5_RX_N	D37	GND
C38	GND	D38	PCIEx8_A_RST
C39	PCIE_x8_slot_B4_RX_P	D39	GND
C40	PCIE_x8_slot_B4_RX_N	D40	PCIEx8_B_RST
C41	GND	D41	GND
C42	PCIE_x8_slot_B3_RX_P	D42	PCIEx8_C_RST
C43	PCIE_x8_slot_B3_RX_N	D43	GND
C44	GND	D44	PCIEx8_D_RST
C45	PCIE_x8_slot_B2_RX_P	D45	GND
C46	PCIE_x8_slot_B2_RX_N	D46	GND
C47	GND	D47	GND
C48	PCIE_x8_slot_B1_RX_P	D48	GND
C49	PCIE_x8_slot_B1_RX_N	D49	GND
C50	GND	D50	GND
C51	PCIE_x8_slot_B0_RX_P	D51	GND
C52	PCIE_x8_slot_B0_RX_N	D52	GND
C53	GND	D53	GND
C54	BMC_SMB_PCIEX8_B_SDA	D54	GND
C55	BMC_SMB_PCIEX8_B_SCL	D55	GND
C56	GND	D56	GND

CN_BP3			
A1	GND	B1	GND
A2	PCIE_x8_slot_C7_TX_P	B2	PCIE_x8_slot_D7_TX_P
A3	PCIE_x8_slot_C7_TX_N	B3	PCIE_x8_slot_D7_TX_N
A4	GND	B4	GND
A5	PCIE_x8_slot_C6_TX_P	B5	PCIE_x8_slot_D6_TX_P
A6	PCIE_x8_slot_C6_TX_N	B6	PCIE_x8_slot_D6_TX_N
A7	GND	B7	GND
A8	PCIE_x8_slot_C5_TX_P	B8	PCIE_x8_slot_D5_TX_P
A9	PCIE_x8_slot_C5_TX_N	B9	PCIE_x8_slot_D5_TX_N
A10	GND	B10	GND
A11	PCIE_x8_slot_C4_TX_P	B11	PCIE_x8_slot_D4_TX_P
A12	PCIE_x8_slot_C4_TX_N	B12	PCIE_x8_slot_D4_TX_N
A13	GND	B13	GND
A14	PCIE_x8_slot_C3_TX_P	B14	PCIE_x8_slot_D3_TX_P
A15	PCIE_x8_slot_C3_TX_N	B15	PCIE_x8_slot_D3_TX_N
A16	GND	B16	GND
A17	PCIE_x8_slot_C2_TX_P	B17	PCIE_x8_slot_D2_TX_P
A18	PCIE_x8_slot_C2_TX_N	B18	PCIE_x8_slot_D2_TX_N
A19	GND	B19	GND
A20	PCIE_x8_slot_C1_TX_P	B20	PCIE_x8_slot_D1_TX_P
A21	PCIE_x8_slot_C1_TX_N	B21	PCIE_x8_slot_D1_TX_N
A22	GND	B22	GND
A23	PCIE_x8_slot_C0_TX_P	B23	PCIE_x8_slot_D0_TX_P
A24	PCIE_x8_slot_C0_TX_N	B24	PCIE_x8_slot_D0_TX_N
A25	GND	B25	GND
A26	CPU0_GPP_CLK03_DP	B26	CPU0_GPP_CLK04_DP
A27	CPU0_GPP_CLK03_DN	B27	CPU0_GPP_CLK04_DN
A28	GND	B28	GND
A29	GND	B29	GND
A30	PCIE_x8_slot_C7_RX_P	B30	PCIE_x8_slot_D7_RX_P
A31	PCIE_x8_slot_C7_RX_N	B31	PCIE_x8_slot_D7_RX_N
A32	GND	B32	GND
A33	PCIE_x8_slot_C6_RX_P	B33	PCIE_x8_slot_D6_RX_P
A34	PCIE_x8_slot_C6_RX_N	B34	PCIE_x8_slot_D6_RX_N
A35	GND	B35	GND
A36	PCIE_x8_slot_C5_RX_P	B36	PCIE_x8_slot_D5_RX_P
A37	PCIE_x8_slot_C5_RX_N	B37	PCIE_x8_slot_D5_RX_N
A38	GND	B38	GND
A39	PCIE_x8_slot_C4_RX_P	B39	PCIE_x8_slot_D4_RX_P
A40	PCIE_x8_slot_C4_RX_N	B40	PCIE_x8_slot_D4_RX_N
A41	GND	B41	GND

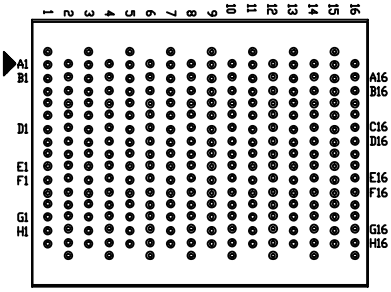
A42	PCIE_x8_slot_C3_RX_P	B42	PCIE_x8_slot_D3_RX_P
A43	PCIE_x8_slot_C3_RX_N	B43	PCIE_x8_slot_D3_RX_N
A44	GND	B44	GND
A45	PCIE_x8_slot_C2_RX_P	B45	PCIE_x8_slot_D2_RX_P
A46	PCIE_x8_slot_C2_RX_N	B46	PCIE_x8_slot_D2_RX_N
A47	GND	B47	GND
A48	PCIE_x8_slot_C1_RX_P	B48	PCIE_x8_slot_D1_RX_P
A49	PCIE_x8_slot_C1_RX_N	B49	PCIE_x8_slot_D1_RX_N
A50	GND	B50	GND
A51	PCIE_x8_slot_C0_RX_P	B51	PCIE_x8_slot_D0_RX_P
A52	PCIE_x8_slot_C0_RX_N	B52	PCIE_x8_slot_D0_RX_N
A53	GND	B53	GND
A54	NC	B54	ND
A55	NC	B55	ND
A56	GND	B56	GND
C1	GND	D1	GND
C2	P0_PCIE_PWRBRK_L	D2	GND
C3	GND	D3	GND
C4	GND	D4	GND
C5	P12V_BP_EN	D5	GND
C6	GND	D6	GND
C7	GND	D7	GND
C8	P12V_FAN_EN	D8	GND
C9	GND	D9	GND
C10	GND	D10	GND
C11	FAN_PWM_EN_MCU	D11	GND
C12	GND	D12	GND
C13	GND	D13	GND
C14	P12V_STBY	D14	GND
C15	P12V_STBY	D15	GND
C16	GND	D16	GND
C17	PCIE_WAKE_N	D17	GND
C18	GND	D18	GND
C19	GND	D19	GND
C20	GND	D20	GND
C21	GND	D21	GND
C22	GND	D22	GND
C23	GND	D23	GND
C24	GND	D24	GND
C25	GND	D25	GND
C26	GND	D26	GND
C27	GND	D27	GND

C41	GND	D41	P3V3_AUX
C42	GND	D42	P3V3_AUX
C43	GND	D43	P3V3_AUX
C44	GND	D44	P3V3_AUX
C45	GND	D45	P3V3_AUX
C46	GND	D46	P3V3_AUX
C47	GND	D47	P3V3_AUX
C48	GND	D48	P3V3_AUX
C49	GND	D49	P3V3_AUX
C50	GND	D50	P3V3_AUX
C51	GND	D51	P3V3_AUX
C52	GND	D52	P3V3_AUX
C53	GND	D53	P3V3_AUX
C54	FPGA_VDD33_ALW	D54	P3V3_AUX
C55	FPGA_VDD33_ALW	D55	P3V3_AUX
C56	GND	D56	P3V3_AUX
C31	GND	D31	P3V3_AUX
C32	GND	D32	P3V3_AUX
C33	GND	D33	P3V3_AUX
C34	GND	D34	P3V3_AUX
C35	GND	D35	P3V3_AUX
C36	GND	D36	P3V3_AUX
C37	GND	D37	P3V3_AUX
C38	GND	D38	P3V3_AUX
C39	GND	D39	P3V3_AUX
C40	GND	D40	P3V3_AUX
C38	GND	D38	P3V3_AUX
C39	GND	D39	P3V3_AUX
C40	GND	D40	P3V3_AUX

2.3.7 CN_BP4 : Board to Board Conn



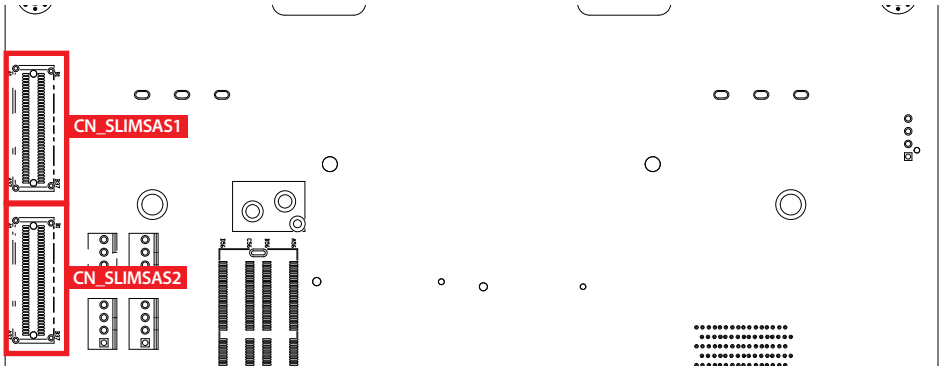
The pin assignments of CPU_PEG_CN1 are listed in the following table :



Pin No.	Function	Pin No.	Function
A1-1	M2A_LED	A1-9	BMC_SMB_M.2+U.2_SDA
B1-1	M2B_LED	B1-9	BMC_SMB_M.2+U.2_SCLK
C1-1	CPU0_GPP_CLK05_DN	C1-9	GND
D1-1	CPU0_GPP_CLK05_DP	D1-9	GND
E1-1	PCIE_M.2_A0_RX_P	E1-9	PCIE_M.2_C0_RX_P
F1-1	PCIE_M.2_A0_RX_N	F1-9	PCIE_M.2_C0_RX_N
G1-1	PCIE_M.2_A0_TX_P	G1-9	PCIE_M.2_C0_TX_P
H1-1	PCIE_M.2_A0_TX_N	H1-9	PCIE_M.2_C0_TX_N
A1-2	M2C_LED	A1-10	P3V3_AUX
B1-2	M2D_LED	B1-10	P3V3_AUX
C1-2	GND	C1-10	GND
D1-2	GND	D1-10	GND
E1-2	PCIE_M.2_A1_RX_P	E1-10	PCIE_M.2_C1_RX_P
F1-2	PCIE_M.2_A1_RX_N	F1-10	PCIE_M.2_C1_RX_N
G1-2	PCIE_M.2_A1_TX_P	G1-10	PCIE_M.2_C1_TX_P
H1-2	PCIE_M.2_A1_TX_N	H1-10	PCIE_M.2_C1_TX_N
A1-3	GND	A1-11	P5V
B1-3	GND	B1-11	P5V
C1-3	GND	C1-11	GND
D1-3	GND	D1-11	GND
E1-3	PCIE_M.2_A2_RX_P	E1-11	PCIE_M.2_C2_RX_P
F1-3	PCIE_M.2_A2_RX_N	F1-11	PCIE_M.2_C2_RX_N
G1-3	PCIE_M.2_A2_TX_P	G1-11	PCIE_M.2_C2_TX_P
H1-3	PCIE_M.2_A2_TX_N	H1-11	PCIE_M.2_C2_TX_N

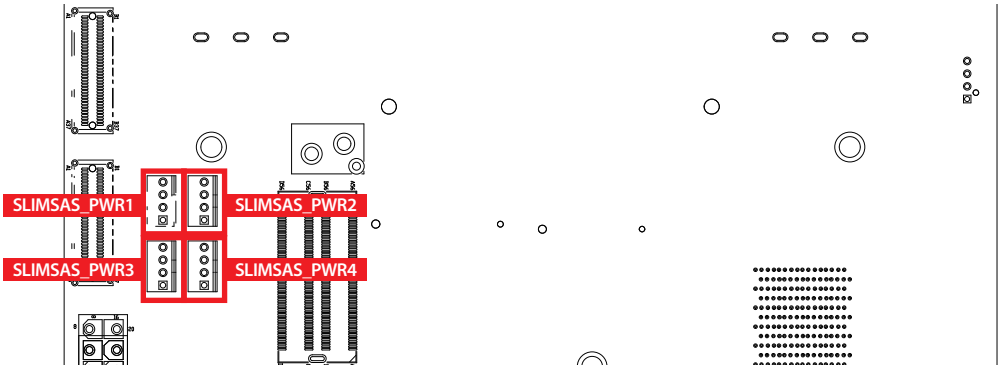
A1-4	GND	A1-12	P12V
B1-4	GND	B1-12	P12V
C1-4	GND	C1-12	GND
D1-4	GND	D1-12	GND
E1-4	PCIE_M.2_A3_RX_P	E1-12	PCIE_M.2_C3_RX_P
F1-4	PCIE_M.2_A3_RX_N	F1-12	PCIE_M.2_C3_RX_N
G1-4	PCIE_M.2_A3_TX_P	G1-12	PCIE_M.2_C3_TX_P
H1-4	PCIE_M.2_A3_TX_N	H1-12	PCIE_M.2_C3_TX_N
A1-5	GND	A1-13	P12V_STBY
B1-5	GND	B1-13	P12V_STBY
C1-5	GND	C1-13	P12V_STBY
D1-5	GND	D1-13	P12V_STBY
E1-5	PCIE_M.2_B0_RX_P	E1-13	PCIE_M.2_D0_RX_P
F1-5	PCIE_M.2_B0_RX_N	F1-13	PCIE_M.2_D0_RX_N
G1-5	PCIE_M.2_B0_TX_P	G1-13	PCIE_M.2_D0_TX_P
H1-5	PCIE_M.2_B0_TX_N	H1-13	PCIE_M.2_D0_TX_N
A1-6	GND	A1-14	P12V_STBY
B1-6	GND	B1-14	P12V_STBY
C1-6	GND	C1-14	P12V_STBY
D1-6	GND	D1-14	P12V_STBY
E1-6	PCIE_M.2_B1_RX_P	E1-14	PCIE_M.2_D1_RX_P
F1-6	PCIE_M.2_B1_RX_N	F1-14	PCIE_M.2_D1_RX_N
G1-6	PCIE_M.2_B1_TX_P	G1-14	PCIE_M.2_D1_TX_P
H1-6	PCIE_M.2_B1_TX_N	H1-14	PCIE_M.2_D1_TX_N
A1-7	P12V_POK_BUF	A1-15	P12V_STBY
B1-7	PERST1_LVC3_N	B1-15	P12V_STBY
C1-7	PCIE_WAKE_N	C1-15	P12V_STBY
D1-7	GND	D1-15	P12V_STBY
E1-7	PCIE_M.2_B2_RX_P	E1-15	PCIE_M.2_D2_RX_P
F1-7	PCIE_M.2_B2_RX_N	F1-15	PCIE_M.2_D2_RX_N
G1-7	PCIE_M.2_B2_TX_P	G1-15	PCIE_M.2_D2_TX_P
H1-7	PCIE_M.2_B2_TX_N	H1-15	PCIE_M.2_D2_TX_N
A1-8	SMB_PCH_SMBDATA	A1-16	P12V_STBY
B1-8	SMB_PCH_SMBCLK	B1-16	P12V_STBY
C1-8	GND	C1-16	P12V_STBY
D1-8	GND	D1-16	P12V_STBY
E1-8	PCIE_M.2_B3_RX_P	E1-16	PCIE_M.2_D3_RX_P
F1-8	PCIE_M.2_B3_RX_N	F1-16	PCIE_M.2_D3_RX_N
G1-8	PCIE_M.2_B3_TX_P	G1-16	PCIE_M.2_D3_TX_P
H1-8	PCIE_M.2_B3_TX_N	H1-16	PCIE_M.2_D3_TX_N

2.3.8 CN_SLIMSAS1, CN_SLIMSAS2 : U.2 Tray SLIMSAS cable connector

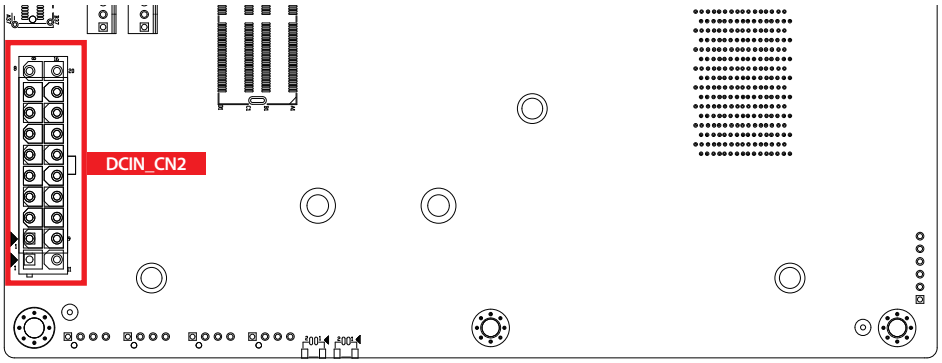


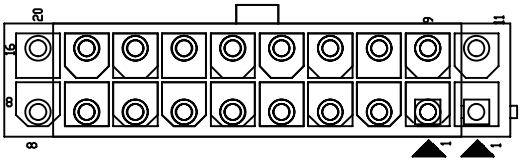
ICS-2000 support front access U.2 tray via cable to connect.

2.3.9 SLIMSAS_PWR1~4 : U.2 Tray power cable connector



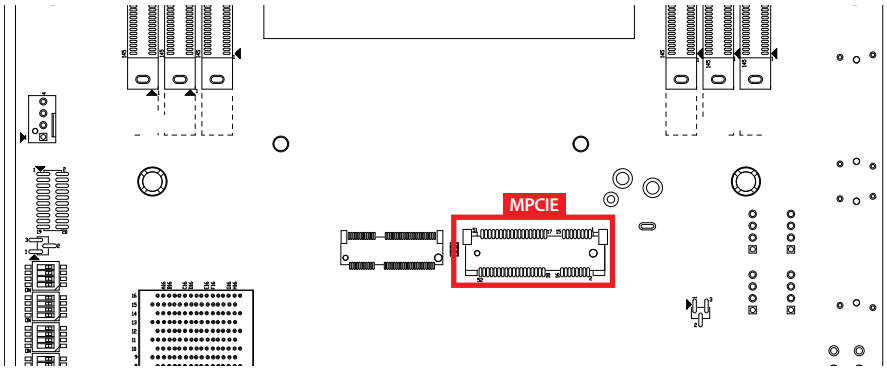
2.3.10 DCIN_CN1 : DC input Connector(12V Only)

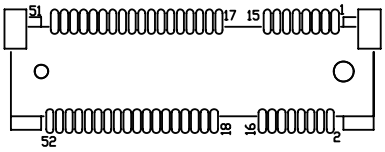




Pin No.	Function	Pin No.	Function
1	V-	9	V-
2	V-	10	V-
3	V-	11	V-
4	V-	12	V-
5	V+	13	V+
6	V+	14	V+
7	V+	15	V+
8	V+	16	V+

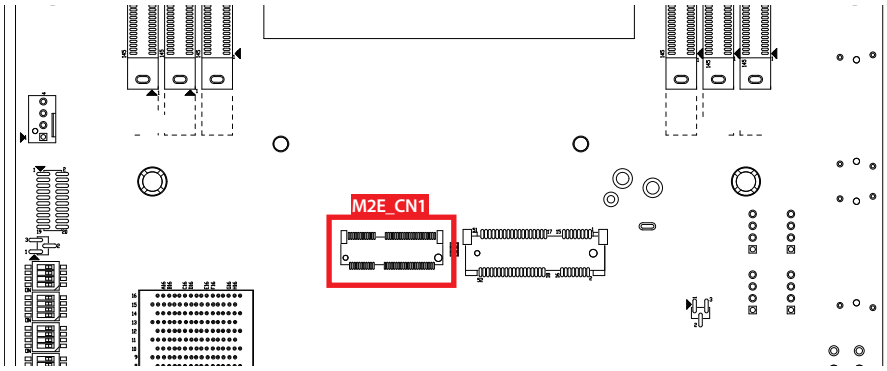
2.3.11 MPCIE1 : Mini PCIe (PCIE Only)

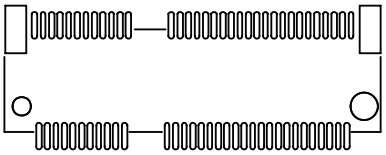




Pin No.	Function	Pin No.	Function
51	Reserved	52	+V3.3A
49	Reserved	50	GND
47	Reserved	48	+1.5V
45	Reserved	46	Reserved
43	Reserved	44	Reserved
41	+V3.3A	42	Reserved
39	+V3.3A	40	GND
37	GND	38	USB_D+
35	GND	36	USB_D-
33	PETp0	34	GND
31	PETn0	32	Reserved
29	GND	30	Reserved
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+V3.3A
21	GND	22	PERST#
19	Reserved	20	reserved
17	Reserved	18	GND
Mechanical Key			
15	GND	16	UIM_VPP_2
13	REFCLK+	14	UIM_RESET_2
11	REFCLK-	12	UIM_CLK_2
9	GND	10	UIM_DATA_2
7	CLKREQ#	8	UIM_PWR_2
5	Reserved	6	1.5V
3	Reserved	4	GND
1	WAKE#	2	+V3.3A

2.3.12 M2E_CN1 : M.2 KEY E USB2, PCIex1 support

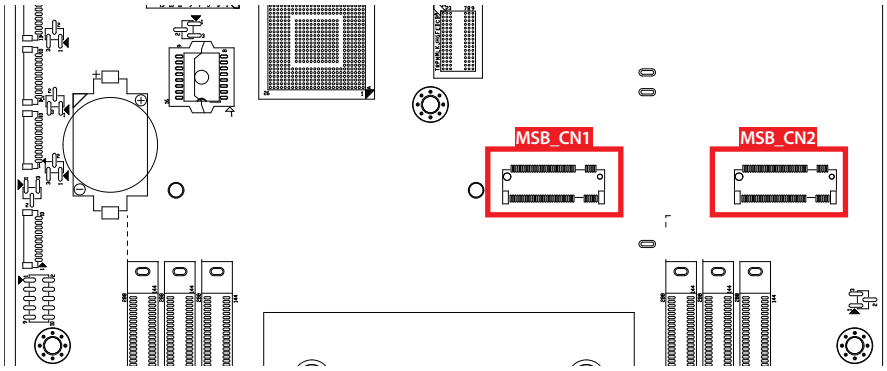




Pin No.	Function	Pin No.	Function
75	GND	74	+V3.3A
73	NC	72	+V3.3A
71	NC	70	NC
69	GND	68	NC
67	NC	66	NC
65	NC	64	NC
63	GND	62	SMB_ALERT#
61	NC	60	SMB_CLK
59	NC	58	SMB_DATA
57	GND	56	NC
55	PCIE_WAKE#	54	NC
53	PCIE_CLK_REQ0#	52	PLTRST#
51	GND	50	NC
49	PCIE_100M_CLK_N0	48	NC
47	PCIE_100M_CLK_P0	46	NC
45	GND	44	NC
43	PCIE_RX_N0	42	NC
41	PCIE_RX_P0	40	NC
39	GND	38	NC
37	PCIE_TX_N0	36	NC
35	PCIE_TX_P0	34	NC
33	GND	32	NC
Mechanical Key			
23	NC		
21	NC	22	NC
19	NC	20	NC
17	NC	18	GND

15	NC	16	NC
13	NC	14	NC
11	NC	12	NC
9	NC	10	NC
7	GND	8	NC
5	USB-	6	LED1#
3	USB+	4	+V3.3A
1	GND	2	+V3.3A

2.3.13 M2B_CN1, M2B_CN2 : M.2 KEY B USB3,USB2,PCIe Support



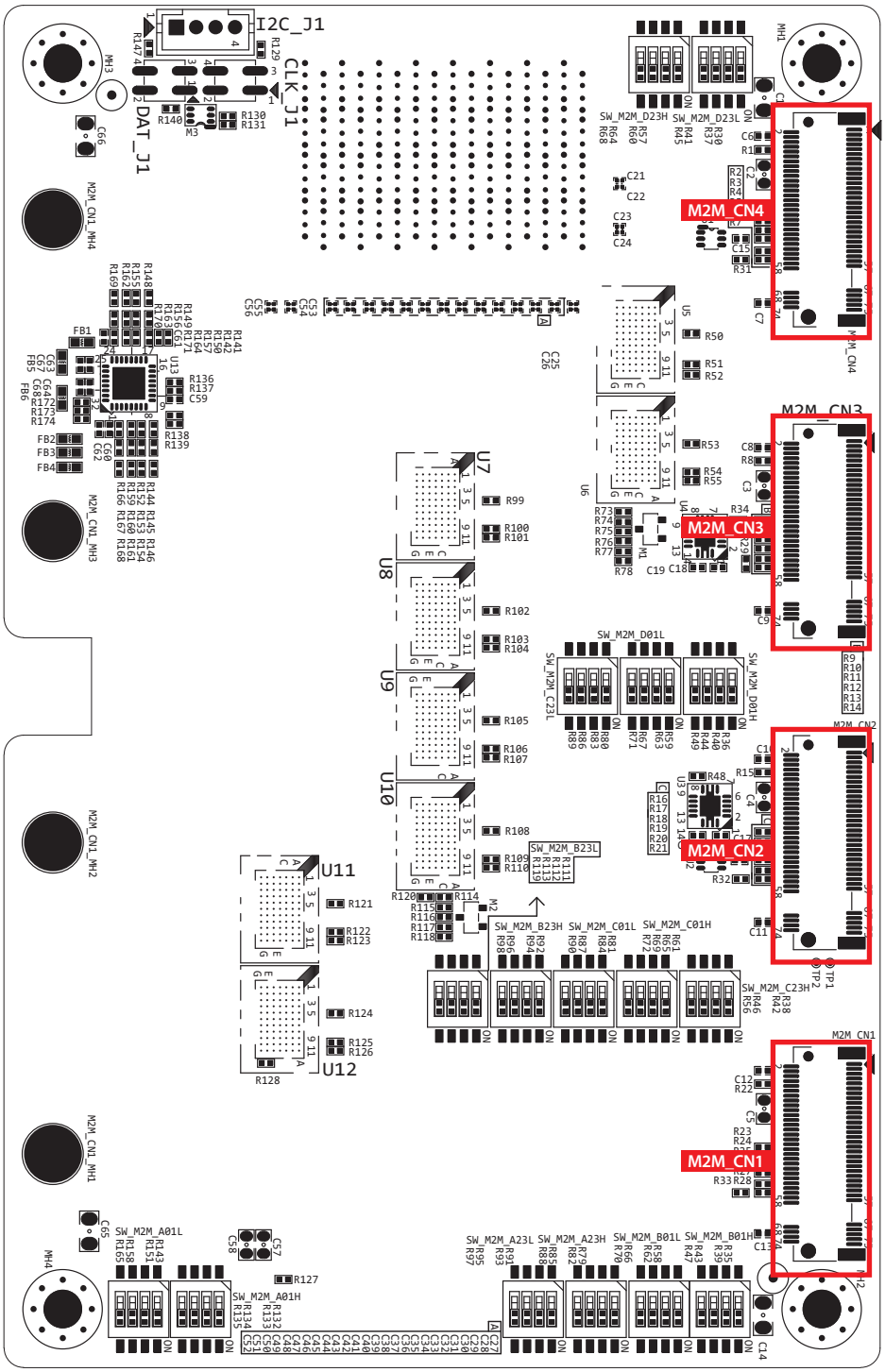
PCIex1 Support(Default) , USB3(BIOS control), Module card types include 3042,3052.
Pin Out :



Pin No.	Function	Pin No.	Function
75	NC	74	+V3.3A
73	GND	72	+V3.3A
71	GND	70	+V3.3A
69	NC	68	NC
67	NC	66	SIM_DETECT
65	NC	64	NC
63	NC	62	NC
61	NC	60	NC
59	NC	58	NC
57	GND	56	NC
55	REFCLKp	54	PCIE_WAKE#
53	REFCLKn	52	PCIE_CLK_REQ
51	GND	50	PLTRST#
49	PETp0	48	NC
47	PETn0,	46	NC
45	GND	44	NC
43	PERp0	42	NC
41	PERn0	40	NC
39	GND	38	DEVSLP
37	USB3.1-TX+	36	UIM_PWR
35	USB3.1-TX-	34	UIM_DATA
33	GND	32	UIM_CLK

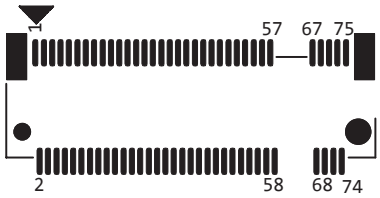
31	USB3.1-RX+	30	UIM_RESET
29	USB3.1-RX-	28	NC
27	GND	26	NC
25	NC	24	NC
23	NC	22	NC
21	NC	20	NC
Mechanical Key			
11	GND		
9	USB-	10	LED1#
7	USB+	8	NC
5	GND	6	FULL_CARD_PWR_OFF
3	GND	4	+V3.3A
1	NC	2	+V3.3A

2.3.14 M2M_CN1~4 : M.2 key M Slot for PCIe x4 Support only (Slot on M2D board)



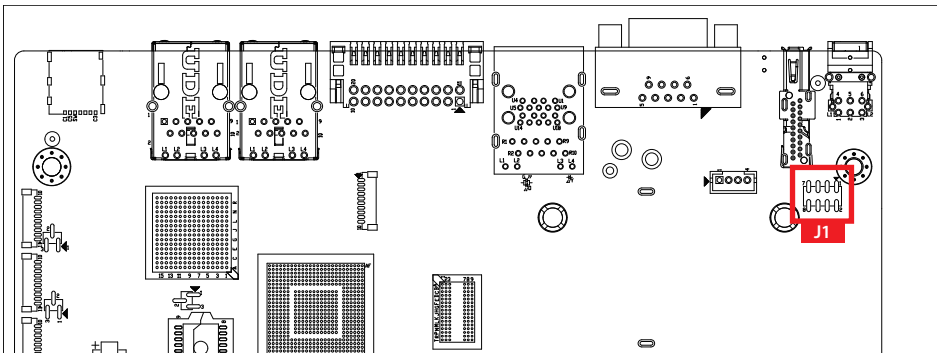
M.2 key M connector is suitable for applications that use Host I/Fs supported by PCIe Module card and types include 2280.

The pin assignments of M2M_CN1~4 are listed in the following table:



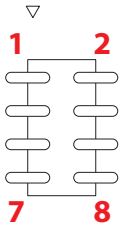
Pin No.	Function	Pin No.	Function
75	GND	74	P3V3_M.2
73	GND	72	P3V3_M.2
71	GND	70	P3V3_M.2
69	NC	68	NC
67	NC		
Mechanical Key			
35	M2M_TX_1N	36	NC
33	GND	34	NC
31	M2M_RX_1P	32	NC
29	M2M_RX_1N	30	NC
27	GND	28	NC
25	M2M_TX_2P	26	NC
23	M2M_TX_2N	24	NC
21	GND	22	NC
19	M2M_RX_2P	20	NC
17	M2M_RX_2N	18	P3V3_M.2
15	GND	16	P3V3_M.2
13	M2M_TX_3P	14	P3V3_M.2
11	M2M_TX_3N	12	P3V3_M.2
9	GND	10	LED1#
7	M2M_RX_3P	8	NC
5	M2M_RX_3N	6	NC
3	GND	4	P3V3_M.2
1	GND	2	P3V3_M.2

2.3.15 J1 : Miscellaneous Pin Header



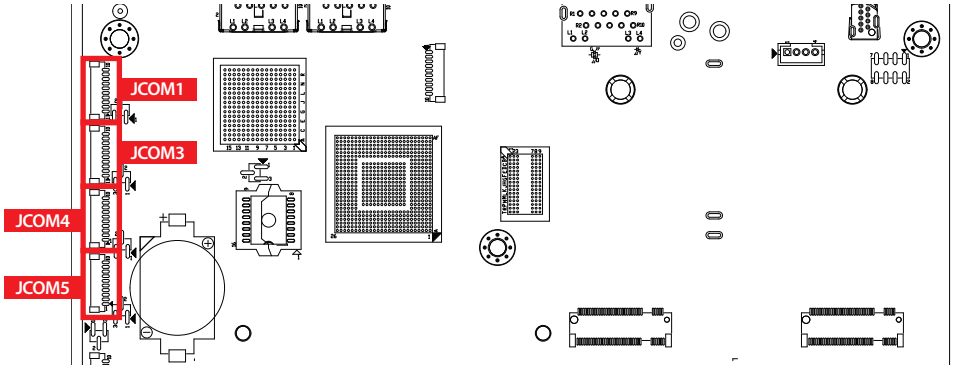
2.0mm 2x4p header
This pin header can be used as a backup for following functions, hard drive LED indicator, reset button, power LED indicator, and power-on/off button.

The pin assignments of J1 are listed in the following table:



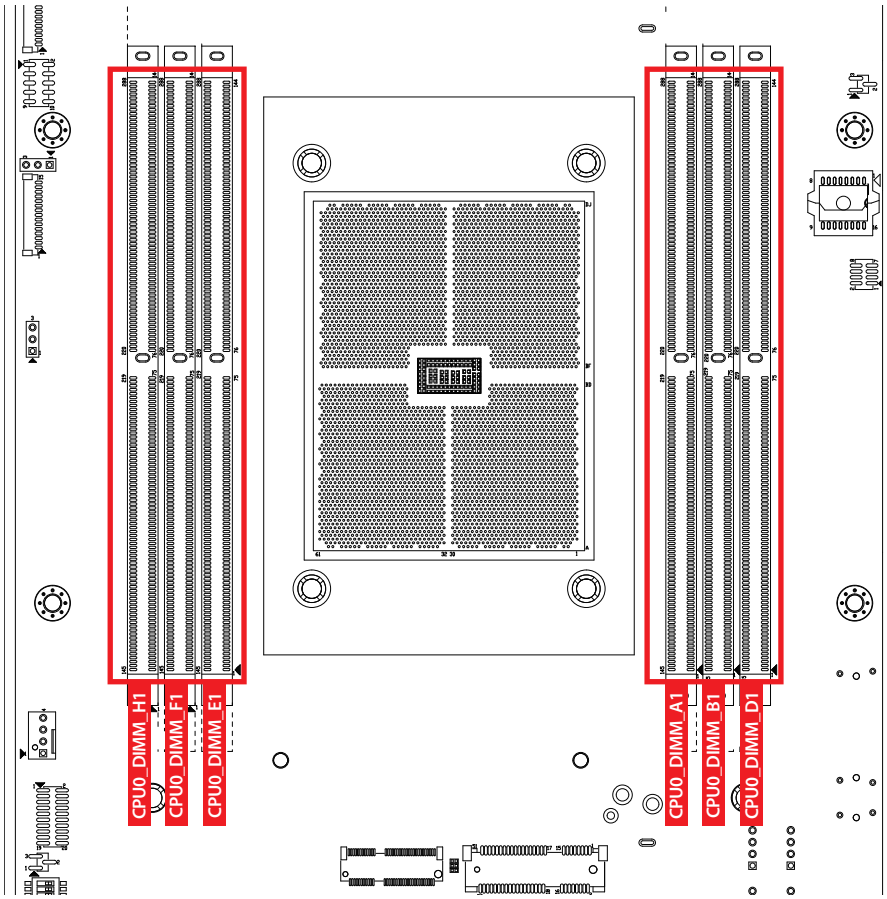
Group	Pin No.	Description
HDD LED	1	HDD_LED_P
	3	HDD_LED_N
RESET BUTTON	5	FP_RST_BTN_N
	7	Ground
POWER LED	2	PWR_LED_P
	4	PWR_LED_N
POWER BUTTON	6	FP_PWR_BTN_IN
	8	Ground

2.3.16 JCOM1, JCOM2, JCOM3, JCOM4 : Serial Port COM Header



ICS-2000 support front access Serial Port COM via cable to connect.

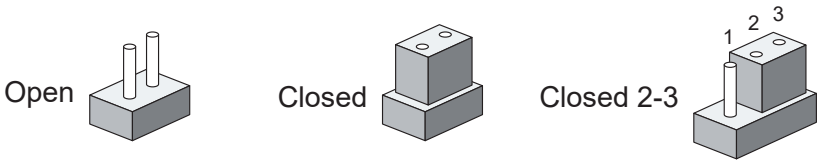
2.3.17 CPU0_DIMM_A1,B1,D1,E1,F1,H1: DDR5 R-DIMM slot



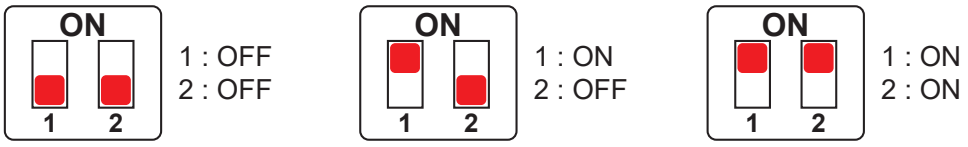
6 DDR5 R-DIMM up to 128GB.

2.4 Main Board Jumper Settings

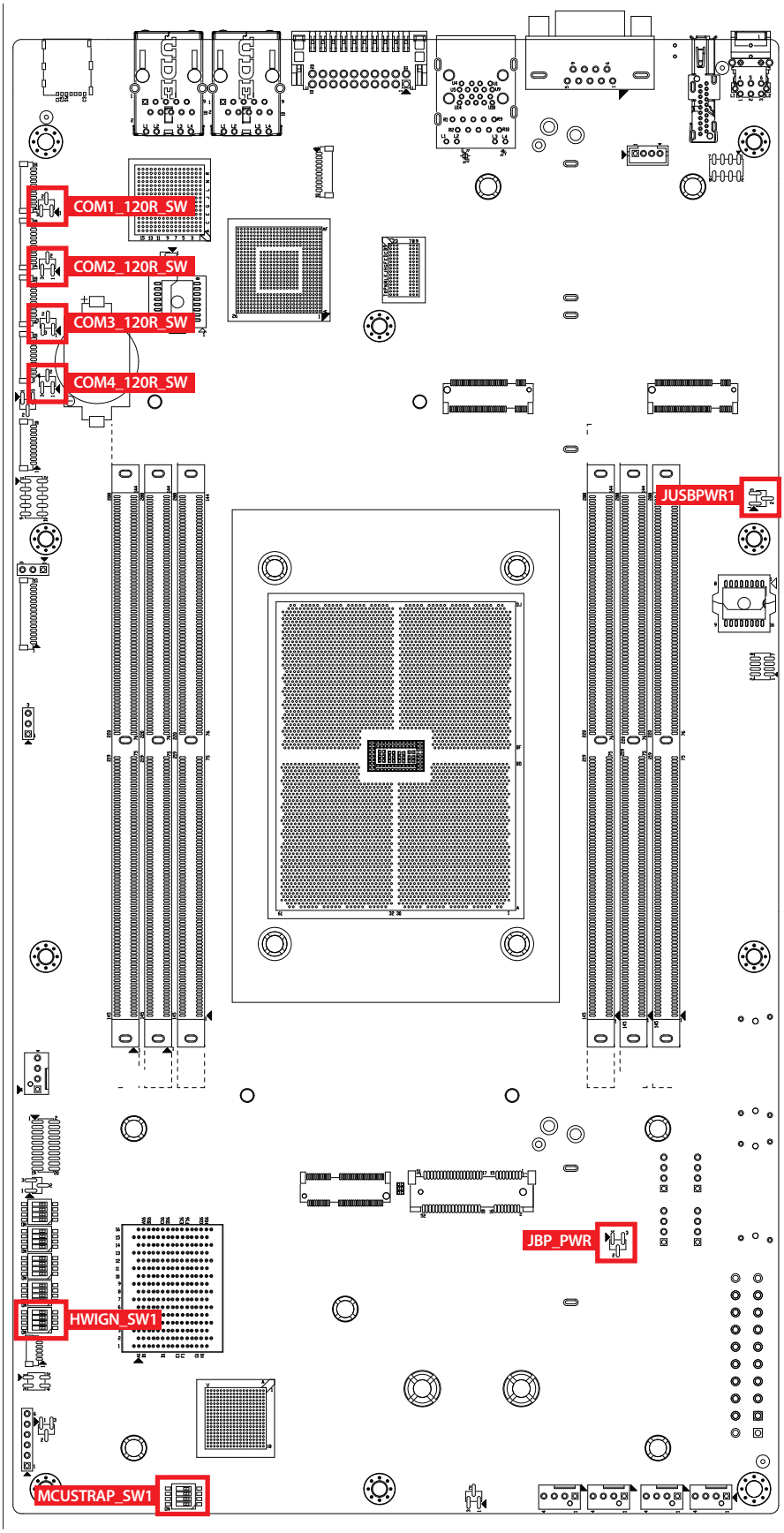
You may configure your card to match the needs of your application by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper, you connect the pins to the clip. To "open" a jumper, you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case you would connect either pins 1 and 2 or 2 and 3.



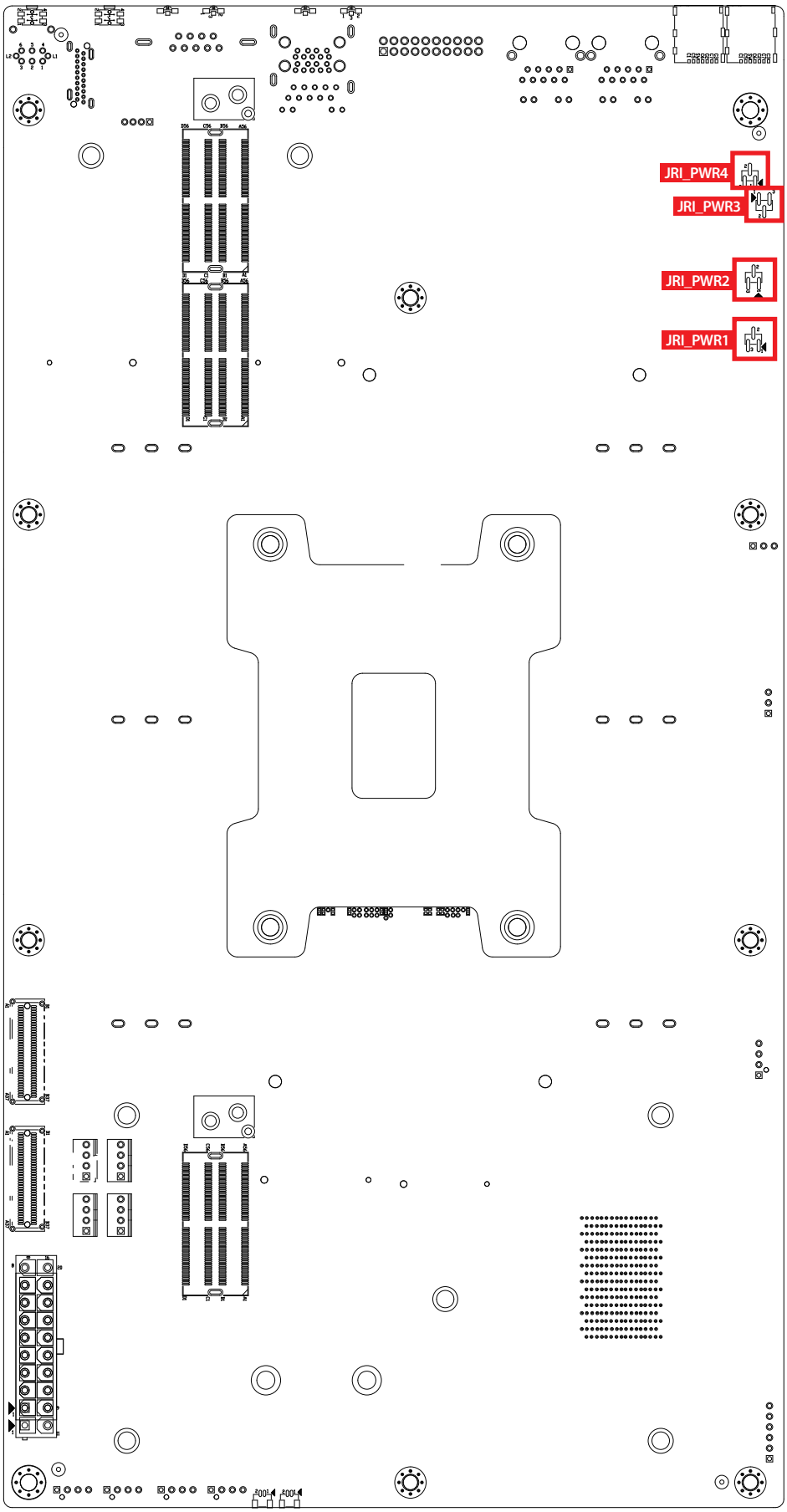
You may configure your card to match the needs of your application by DIP switch. As below show the DIP switch on and off.



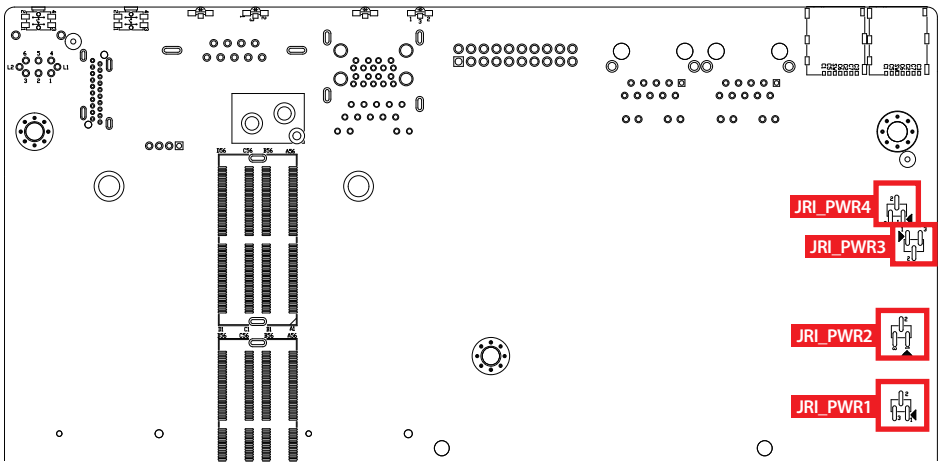
2.4.1 TOP View of ICS-2000 Main Board With Jumper and Tact switch Location

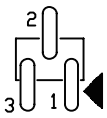


2.4.2 BOTTOM View of ICS-2000 Main Board With Jumper Location



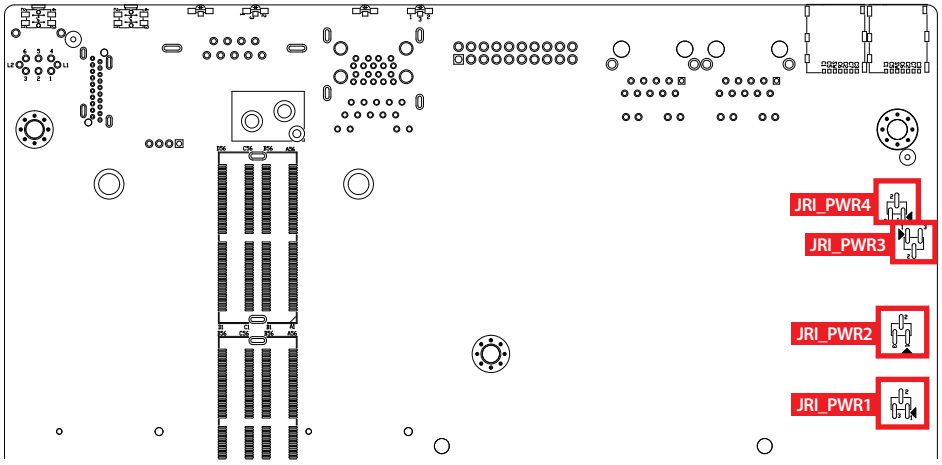
2.4.3 JRI_PWR1~4 : COM1~4 RI Pin Function

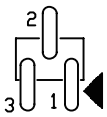




Port	Setting	Description
COM1~4	1 - 2	+12V (0.5A max.)
	2 - 3	RI(Default)

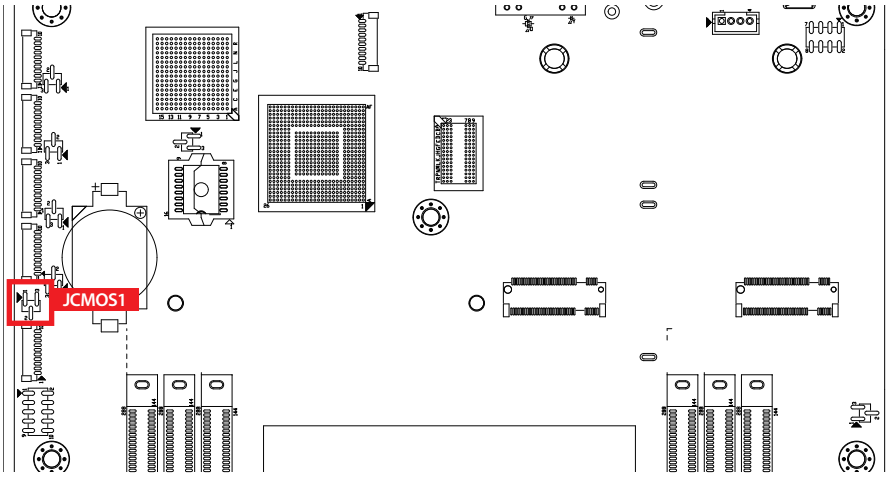
2.4.4 COM1~4_120R_SW : RS-485 RECEIVER TERMINATION RESISTANCE

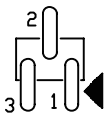




Port	Setting	Description
COM1~4	1 - 2	DCD / RXD Termination 120R disable(default)
	2 - 3	DCD / RXD Termination 120R enable

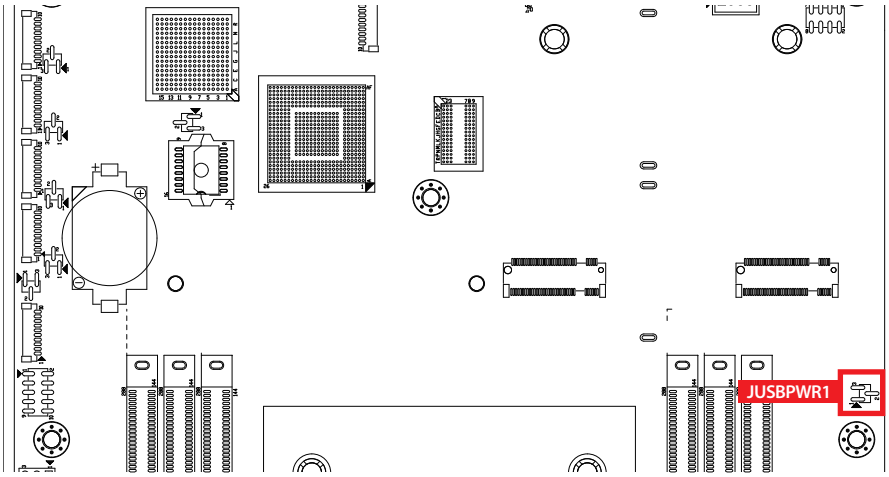
2.4.5 JCMOS1 : Clear CMOS

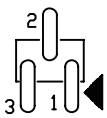




Setting	Description
1 - 2	Normal (Default)
2 - 3	Clear CMOS

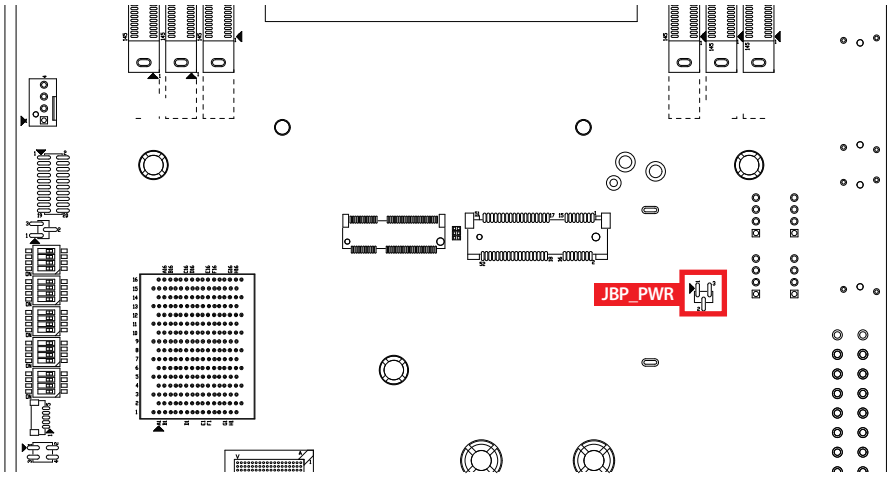
2.4.6 JUSBPWR1 : USB Wake Up

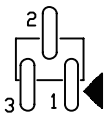




Setting	Description
1 - 2	USB 3.0 and USB 2.0 Wake Up Enable (Default)
2 - 3	USB 3.0 and USB 2.0 Wake Up Disable

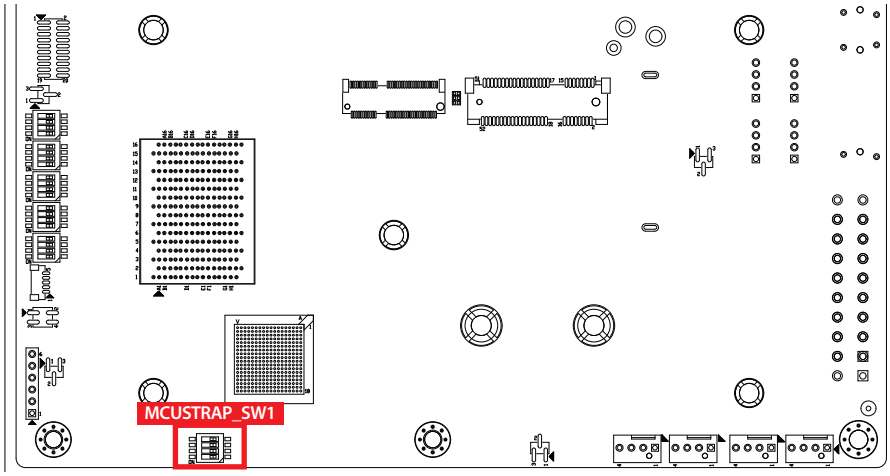
2.4.7 JBP_PWR : Power select for back plane board +12V_BP

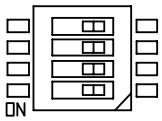




Setting	Description
1 - 2	+12V _BP = System Power (Default)
2 - 3	+12V _BP = Standby Power

2.4.8 MCUSTRAP_SW1 : IGN Mode

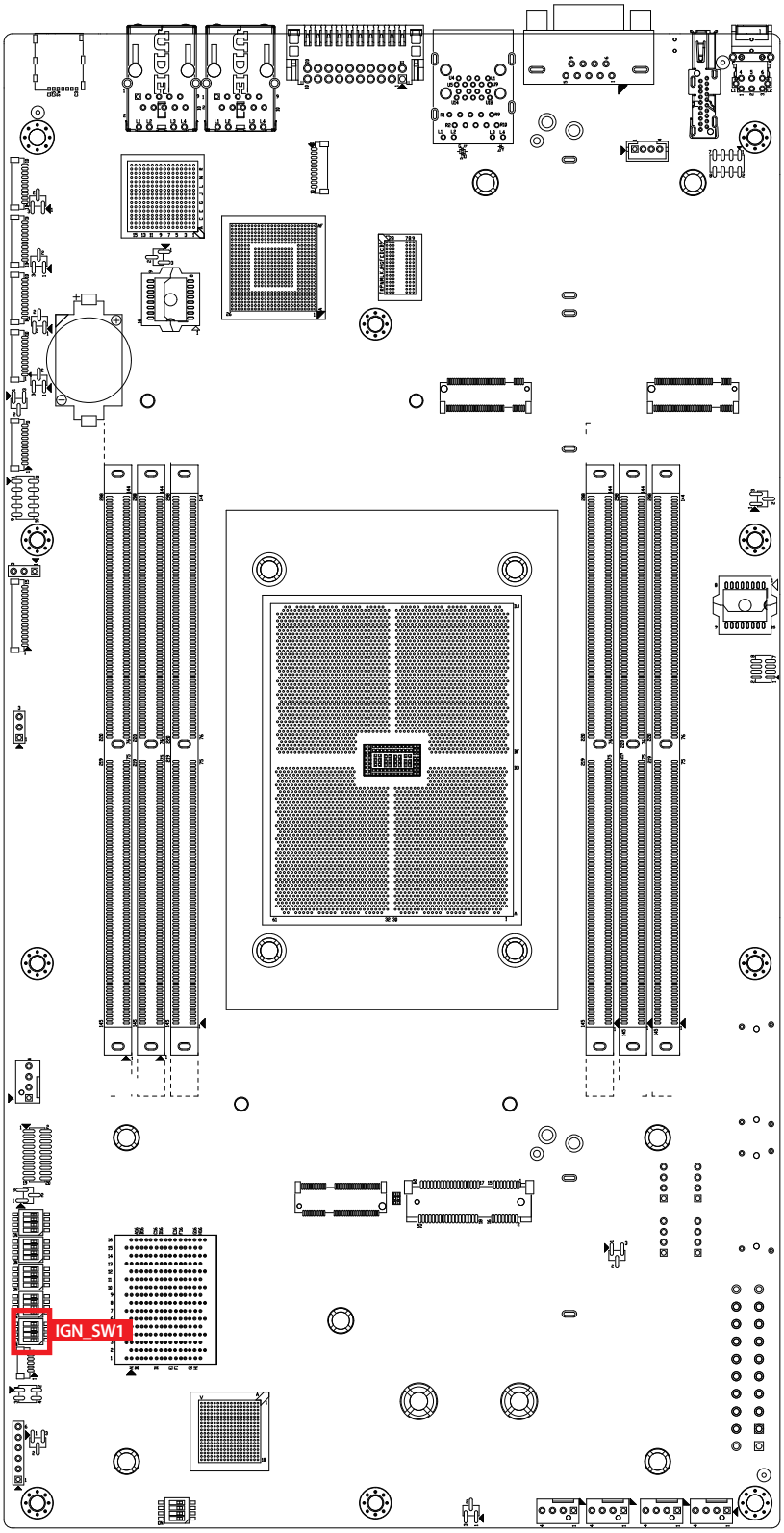




Setting	Description
1 & 2	Must keep OFF status
2 - 3	Off = SW Mode (Default) ON = HW mode
4	NC

2.5 Ignition Control

2.5.1 IGN_SW1 : Ignition Control (HW)

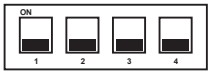
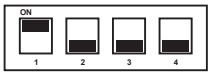
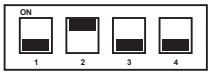
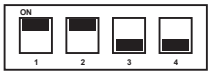
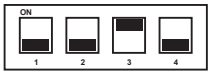
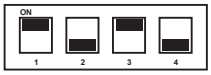
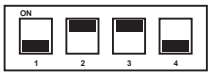
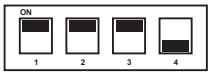
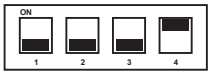
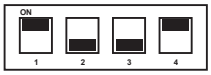
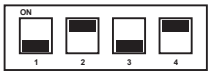
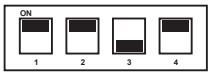
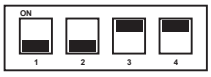
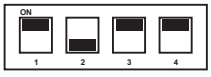
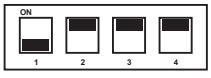
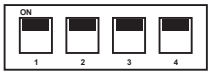


The ICS-2000 provide ignition power control feature for in-vehicle applications. The built-in MCU monitors the ignition signal and turns on/off the system according to pre-defined on/off delay period.

2.5.2 Adjust Ignition Control Modes

The ICS-2000 provide sixteen modes of different power on/off delay periods adjustable via rotary switch. The default rotary switch is set to 0 in ATX/ AT power mode.

The modes are listed in the following table :

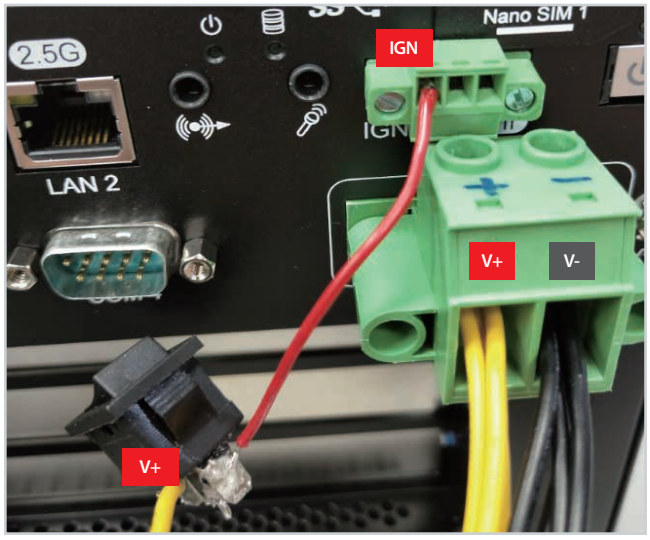
DIP Switch Position	Power On delay	Power Off Delay	Switch Position
0	ATX/AT mode (Default)		
1	No delay	No delay	
2	No delay	5 seconds	
3	No delay	10 seconds	
4	No delay	30 seconds	
5	No delay	60 seconds	
6	5 seconds	10 seconds	
7	5 seconds	30 seconds	
8	5 seconds	60 seconds	
9	5 seconds	90 seconds	
A	5 seconds	120 seconds	
B	10 seconds	10 seconds	
C	10 seconds	30 seconds	
D	10 seconds	60 seconds	
E	10 seconds	90 seconds	
F	10 seconds	120 seconds	

2.5.3 Ignition Control Wiring

To activate ignition control, you need to provide IGN signal via the 3-pin plugable terminal block located on the front panel. Please use the following pictures to find the general wiring configuration.



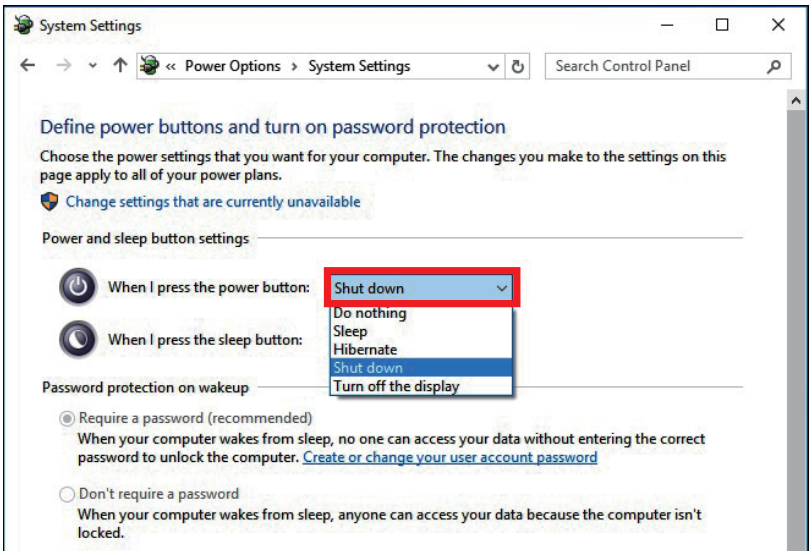
Pin No.	Definition
1	Ignition
2	SW+
3	SW-



For testing purpose, you can refer to the picture blow to simulate ignition signal input controlled by a latching switch.

Note :

1. DC power source and IGN share the same ground.
2. ICS-2000 supports 16V to 50V wide range DC power input in ATX/AT mode.
3. For proper ignition control, the power button setting should be "Power Down" mode.



In Windows for example, you need to set "When I press the power button" to Shut down.

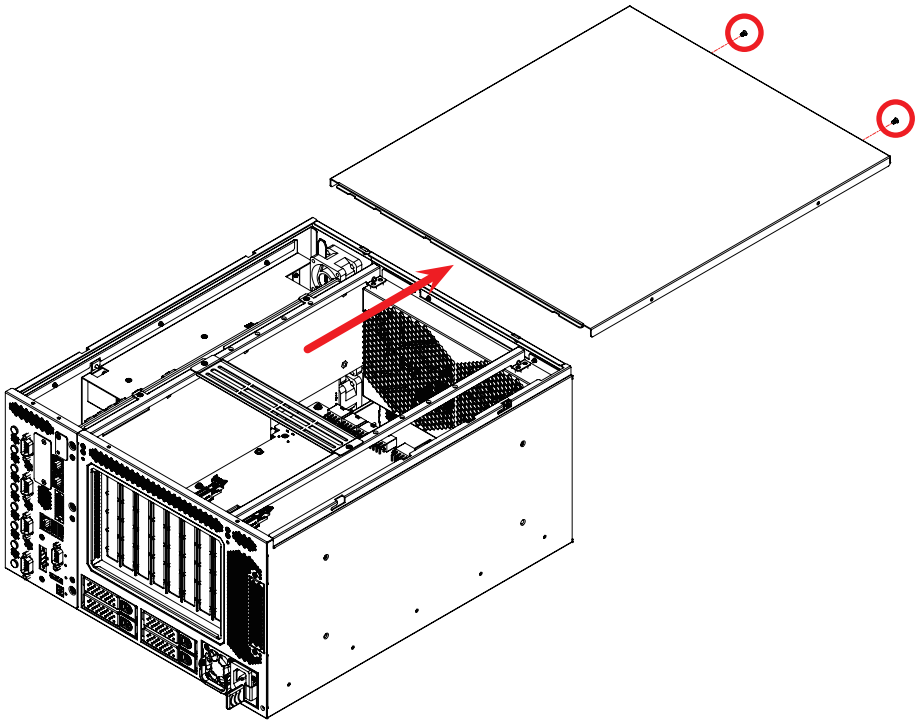
3

SYSTEM SETUP

3.1 How to open your ICS-2000

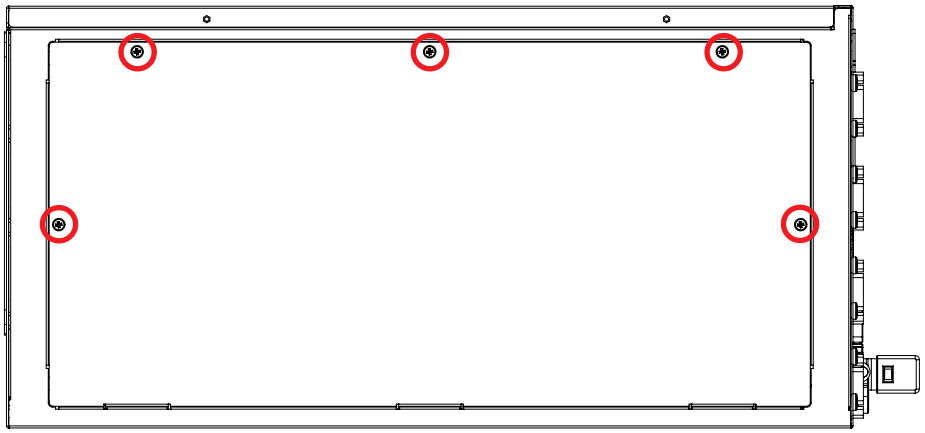
3.1.1 ICS-2000 Series

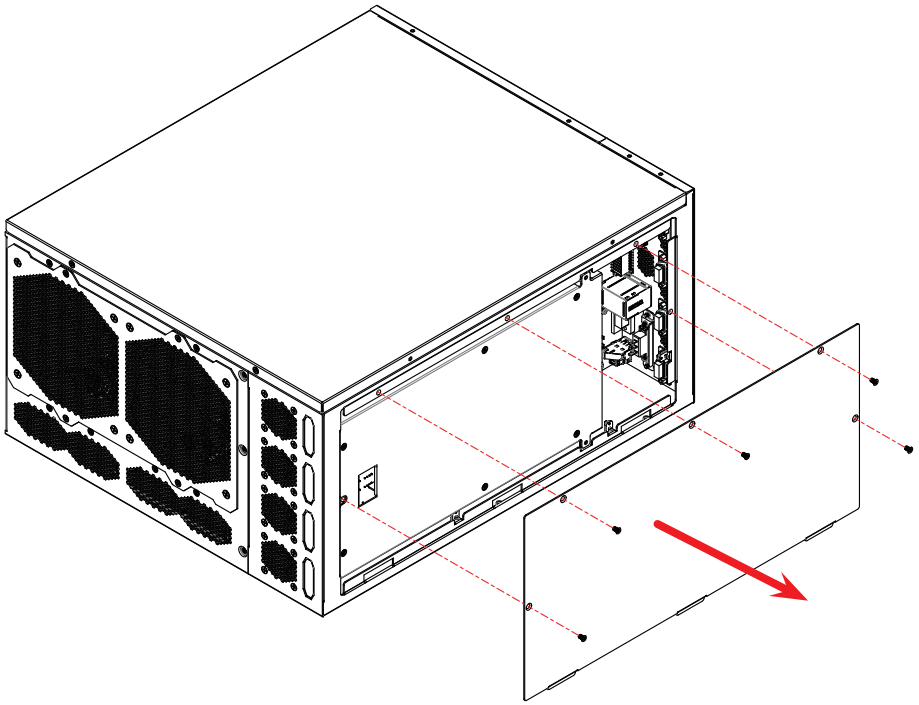
Remove two flat head M3x5L screws and top cover.



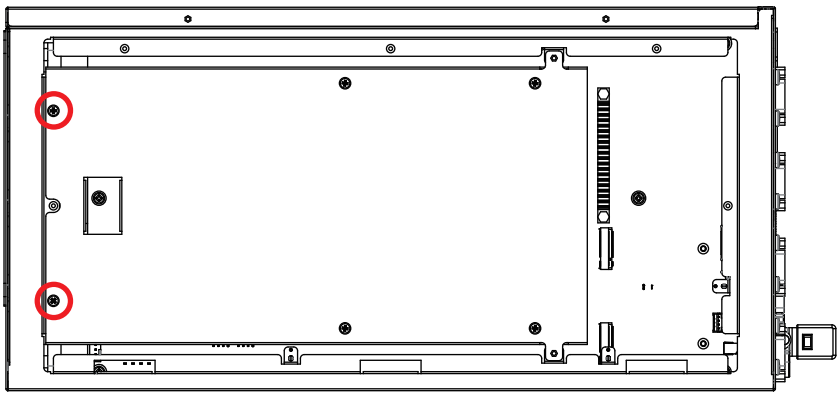
3.2 Installing CPU

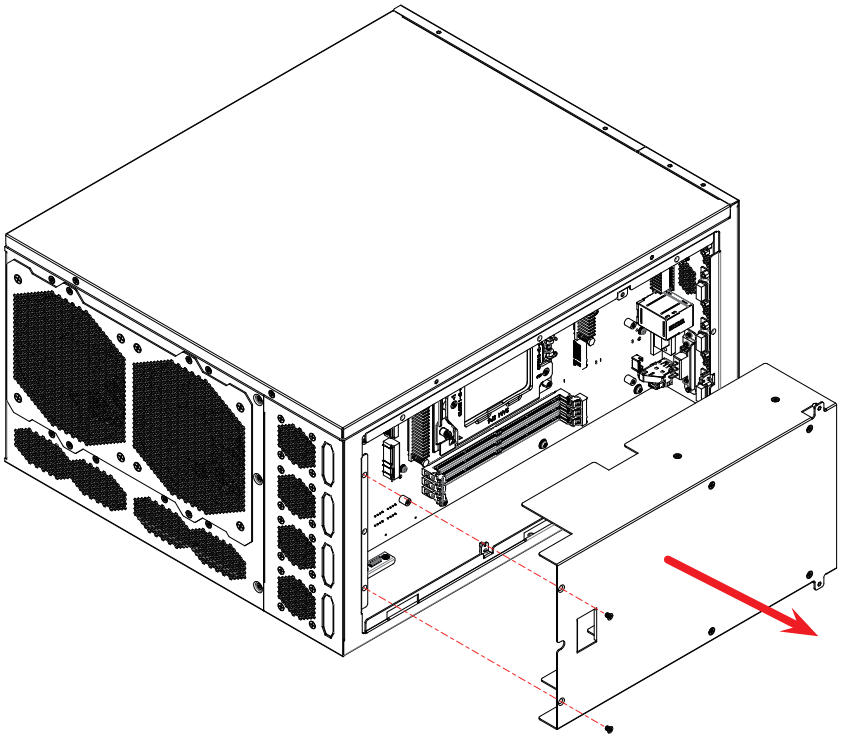
Step 1 Remove five flat head M3x5L screws and side cover.



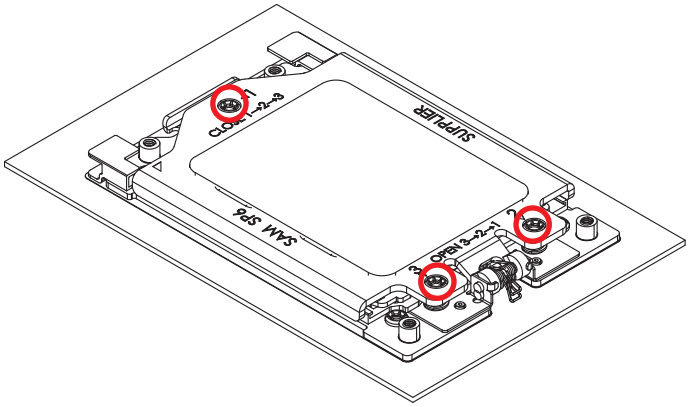


Step 2 Remove two flat head M3x5L screws and air duct.

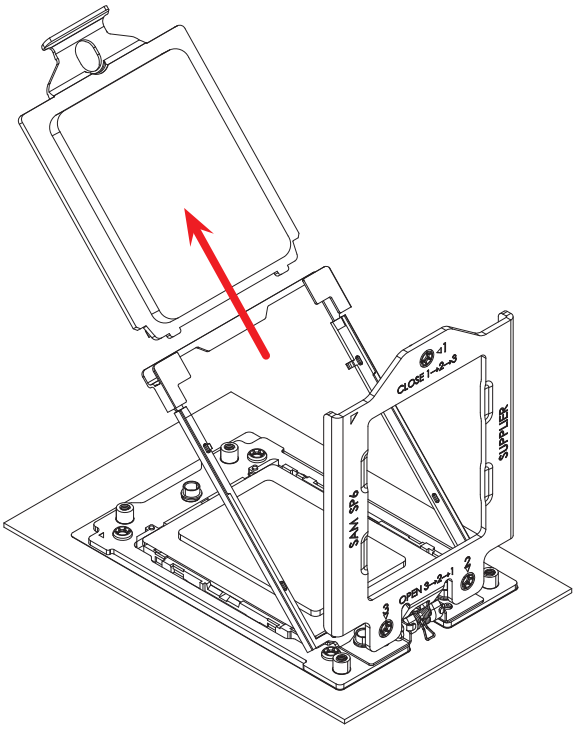




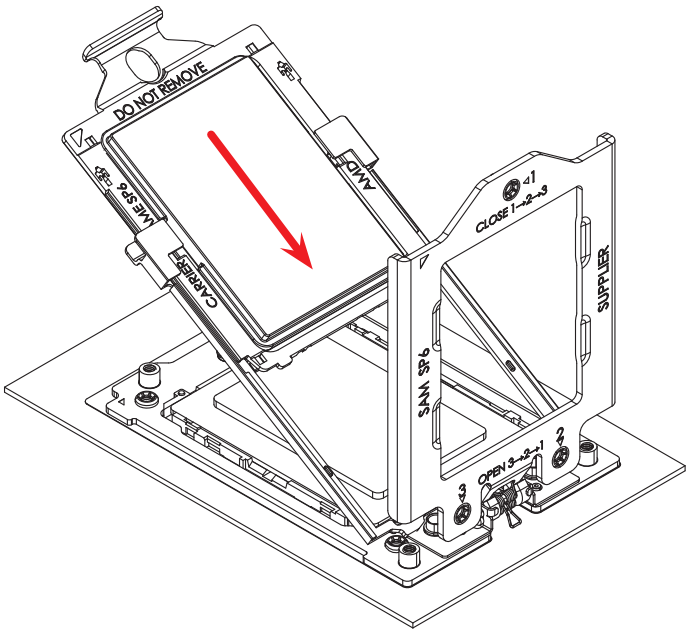
Step 3 Remove CPU socket screw.



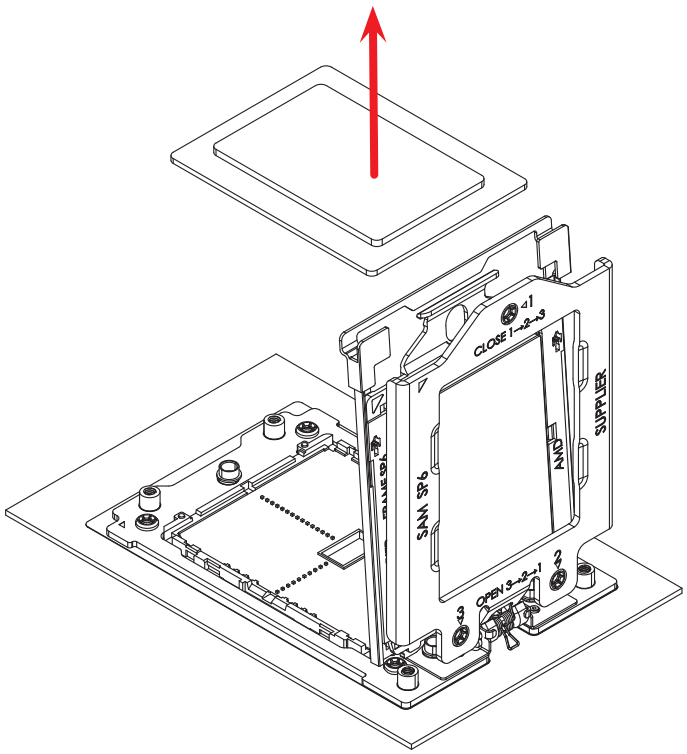
Step 4 Remove CPU dummy bracket.



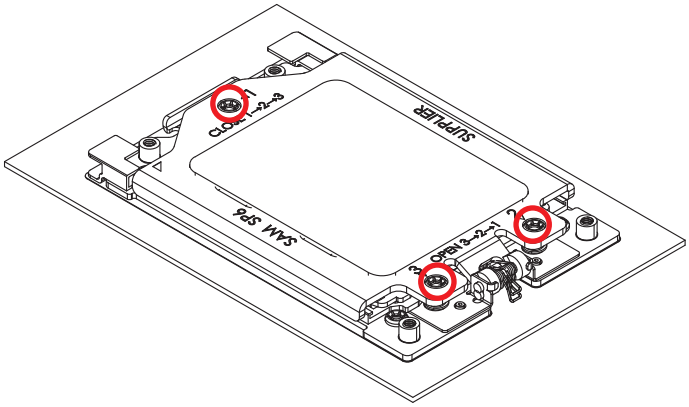
Step 5 Install CPU.



Step 6 Remove CPU socket cover.

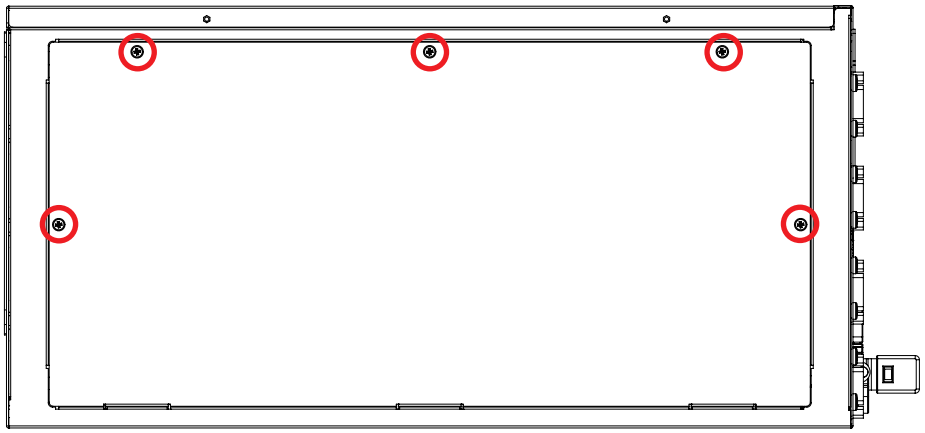


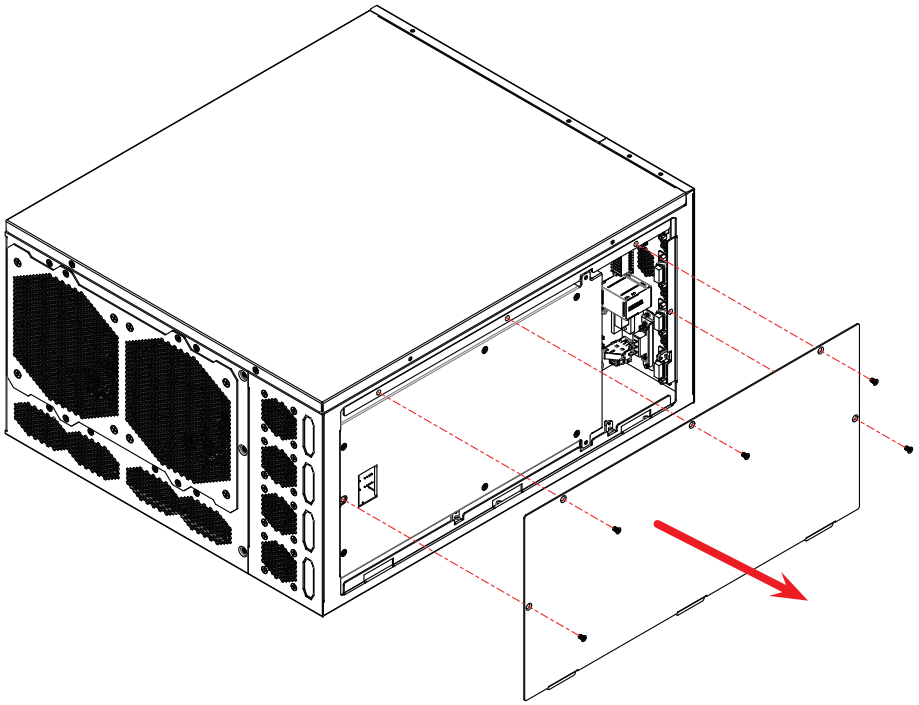
Step 7 Close CPU independent loading mechanism and install screw.



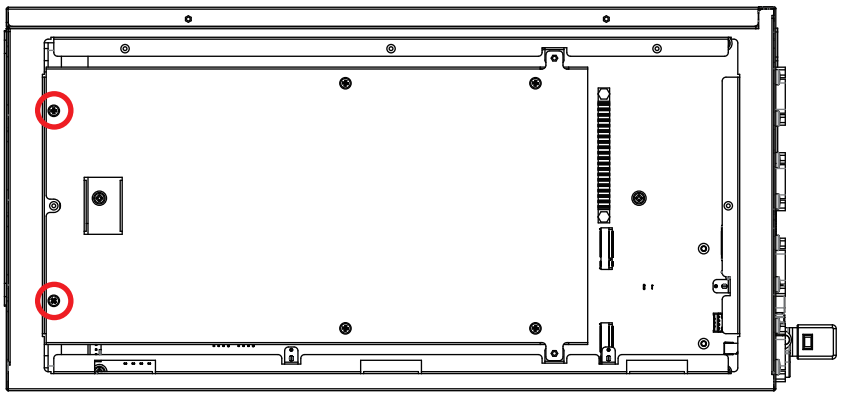
3.3 Installing DDR5 UDIMM Modules

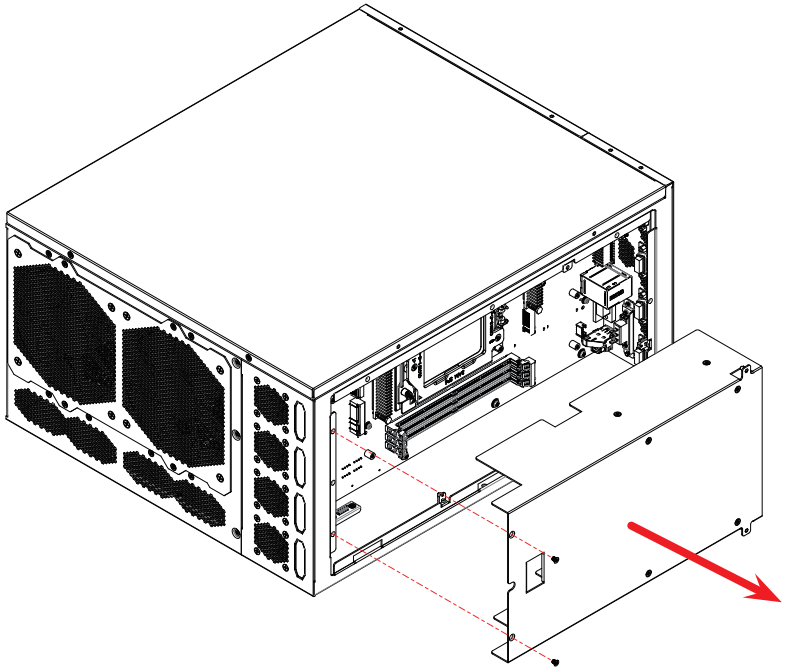
Step 1 Remove five flat head M3x5L screws and side cover.



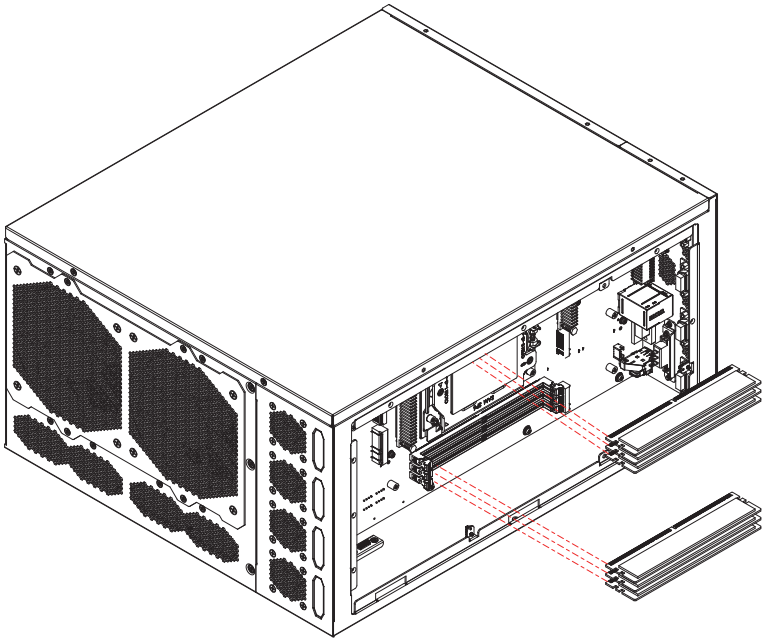


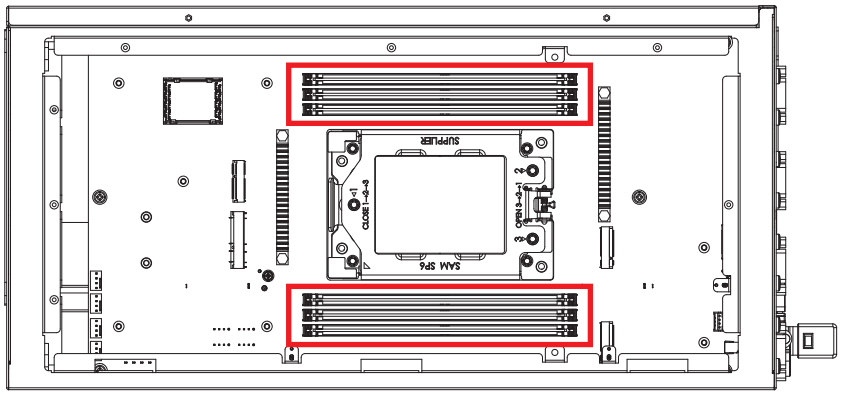
Step 2 Remove two flat head M3x5L screws and air duct.





Step 3 Install DDR5 UDIMM module.



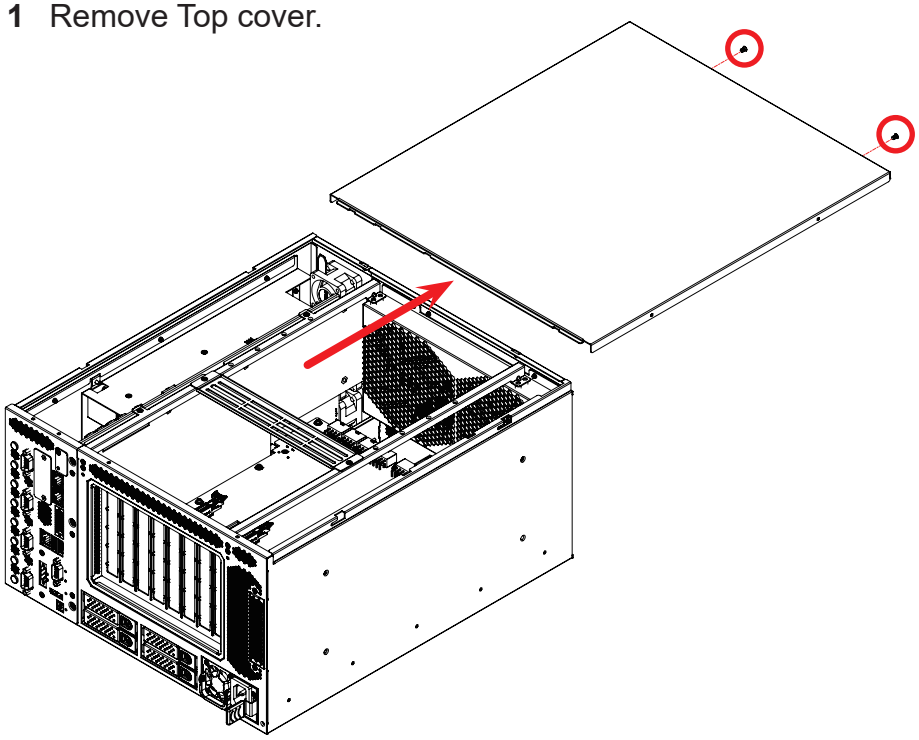


3.4 Installing PCIe Card

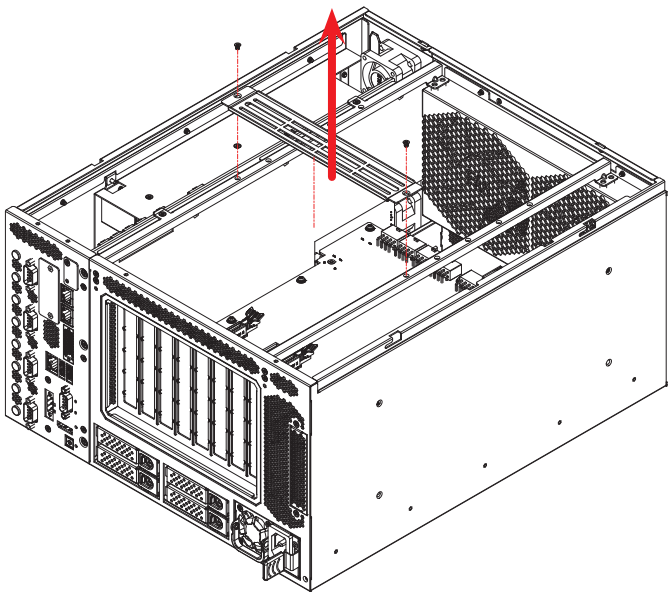
System designs will support 111.15 mm standard height, 312 mm maximum length (without the I/O bracket & power cable) expansion cards.

(*Based on the position of power connectors and the card sink/case design, not all expansion card within the maximum dimension can fit in to the system. Please consult the Vecow support team for confirmation.)

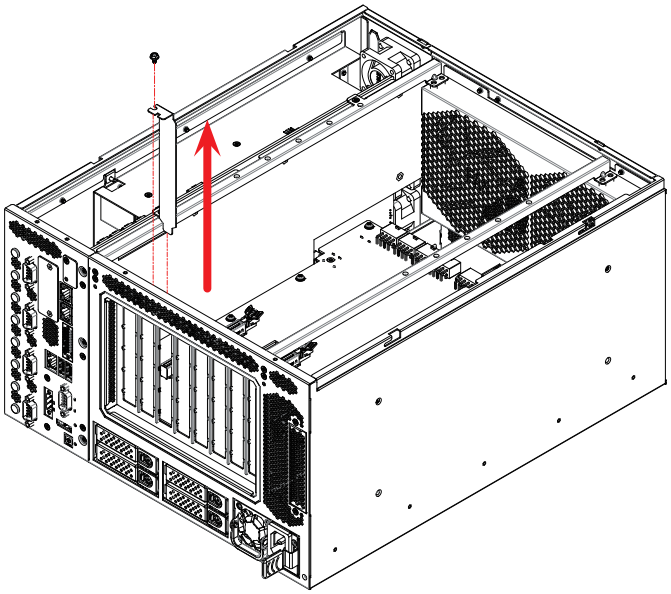
Step 1 Remove Top cover.



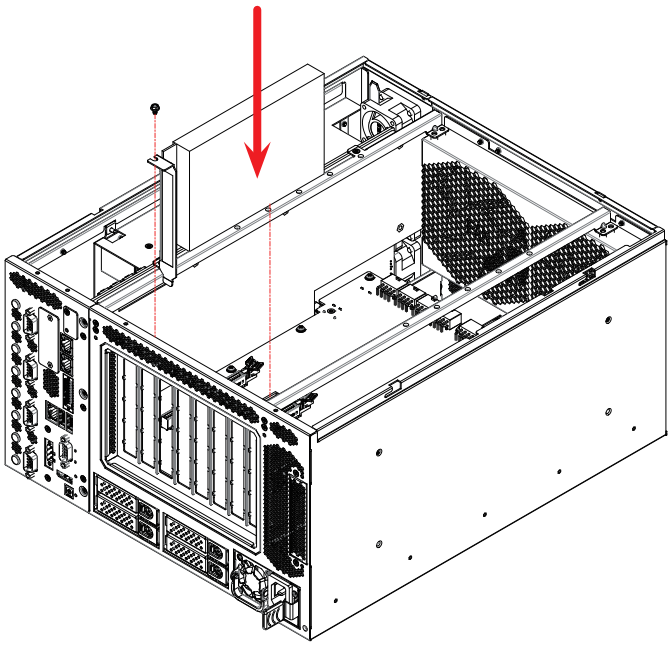
Step 2 Remove two flat head M3x4L and hold down bar bracket.



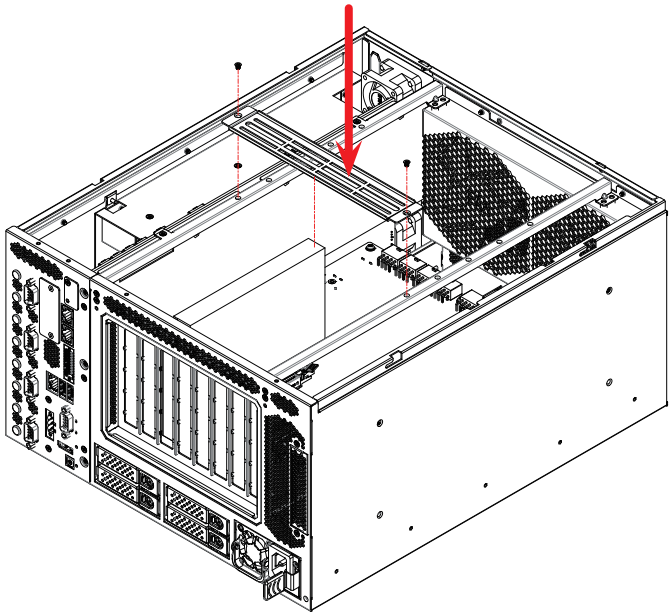
Step 3 Remove one hex head M3x6L and PCIe bracket.

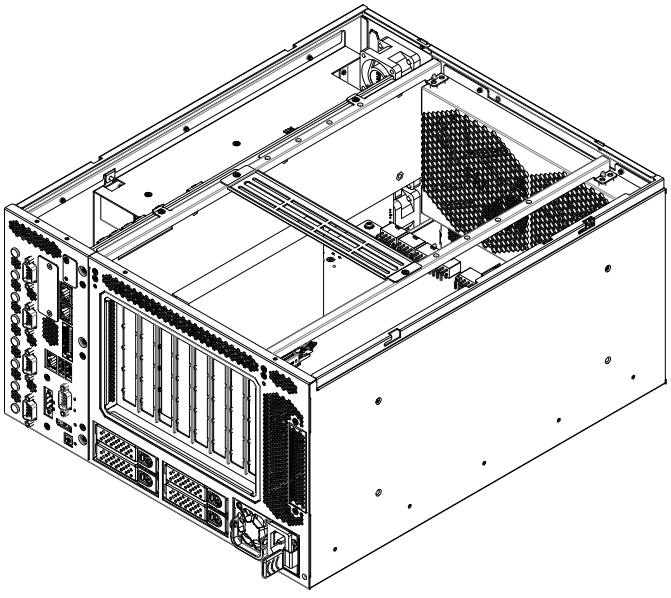


Step 4 Install one hex head M3x6L and PCIe card.



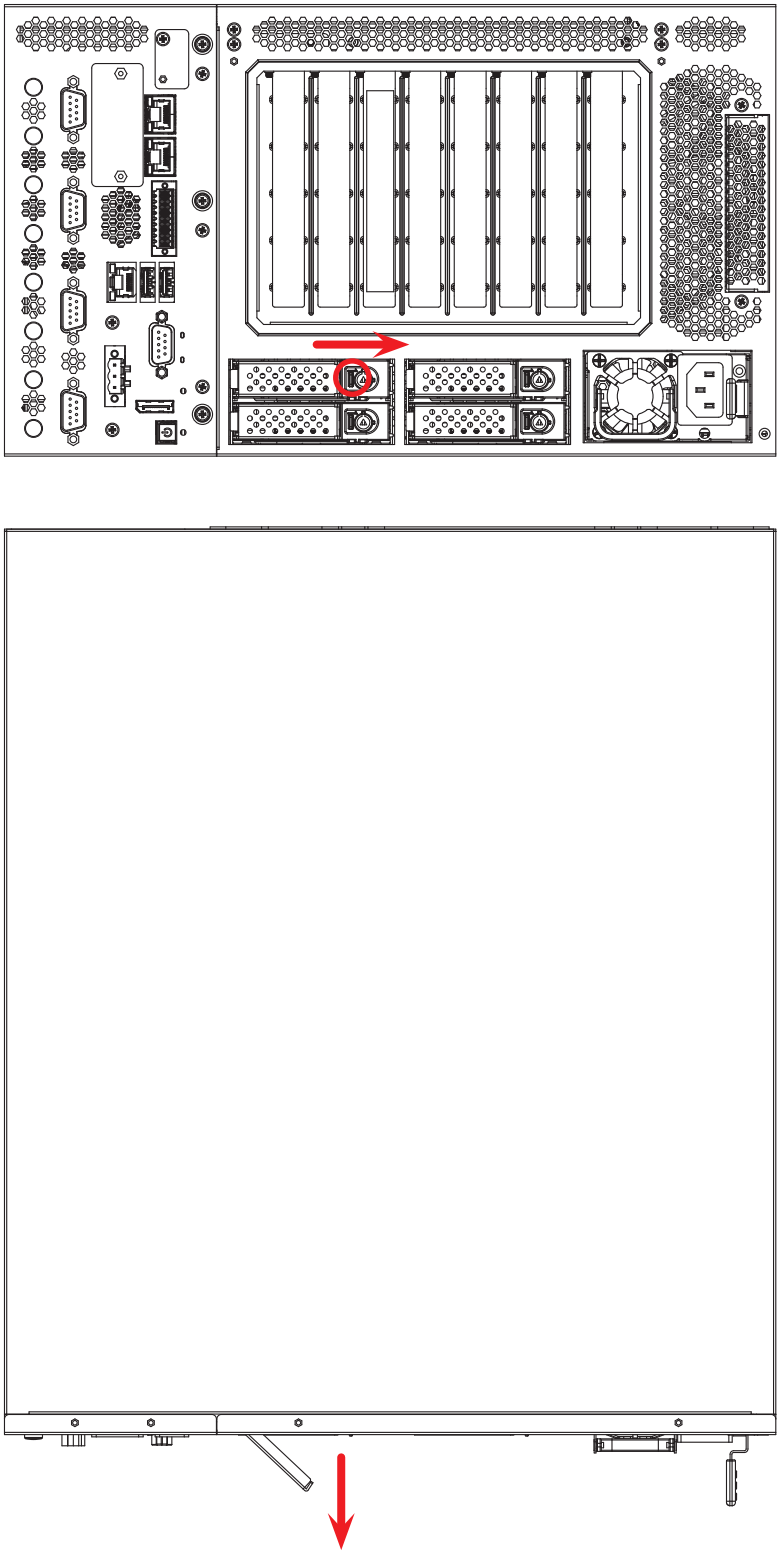
Step 5 Install two flat head M3x4L and hold down bar bracket.



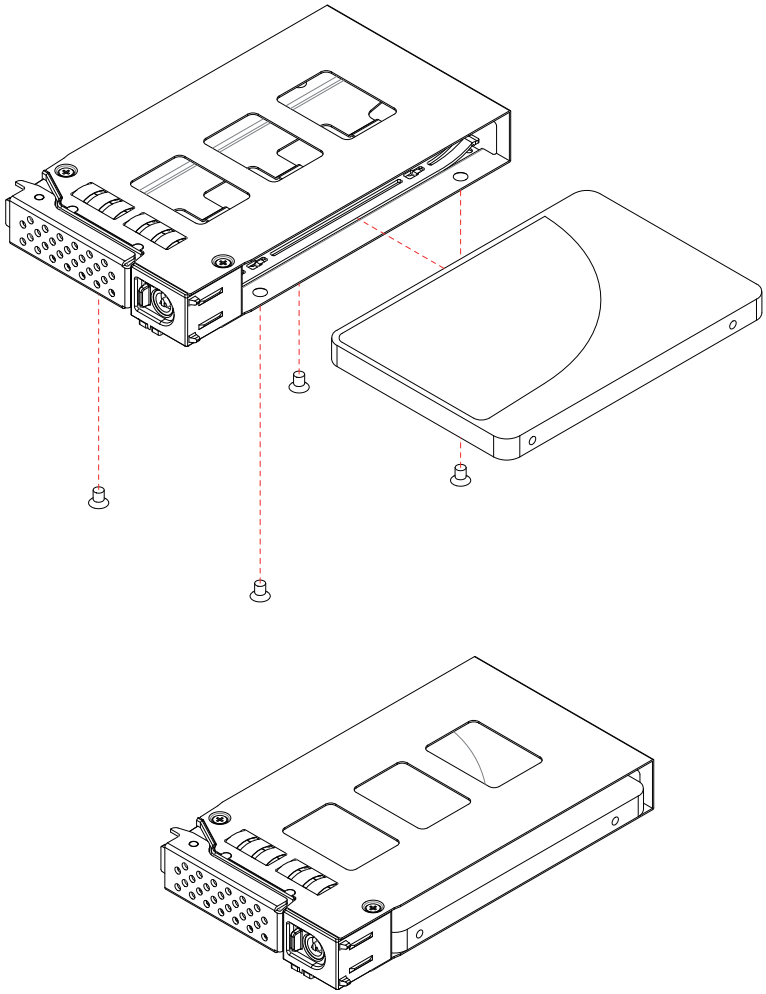


3.5 Installing U.2

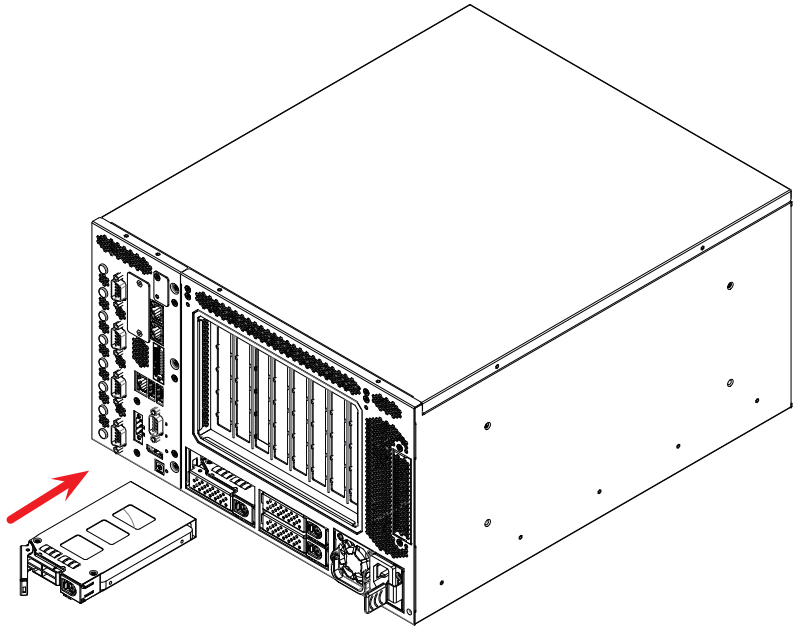
Step 1 Remove 8 M3 flat head screws and remove the top cover.

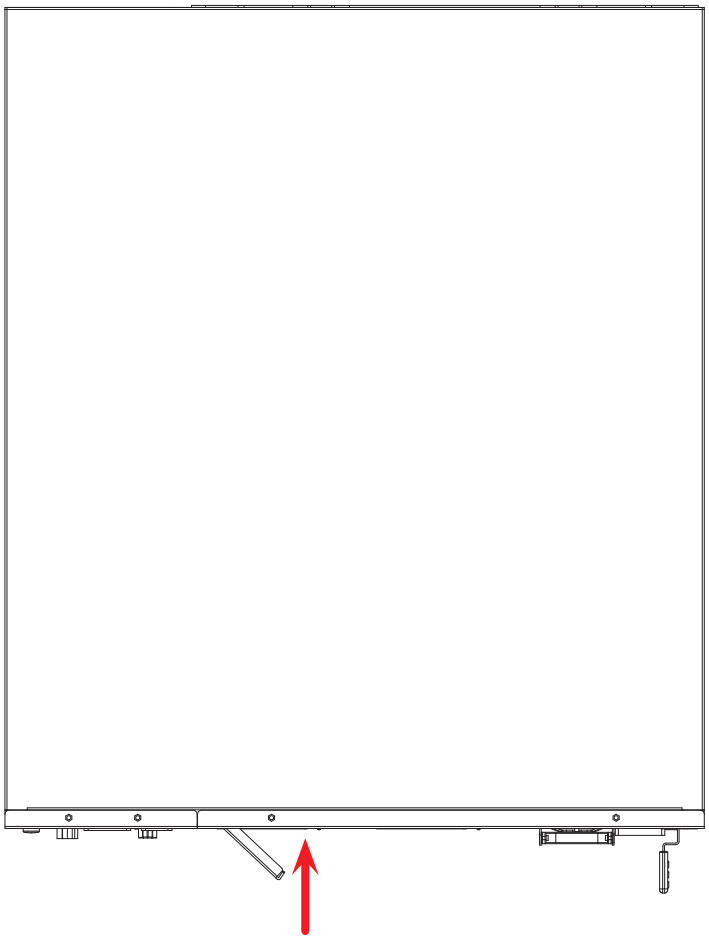


Step 2 Install U.2 into the tray.

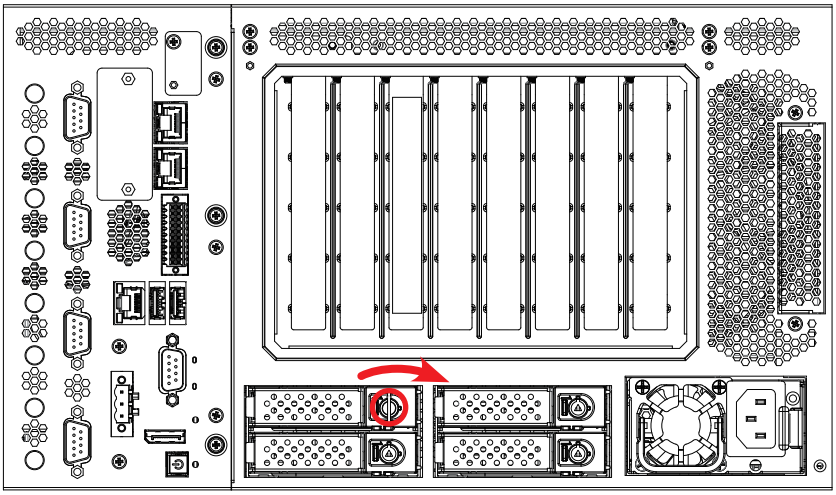


Step 3 Install U.2 tray and close.



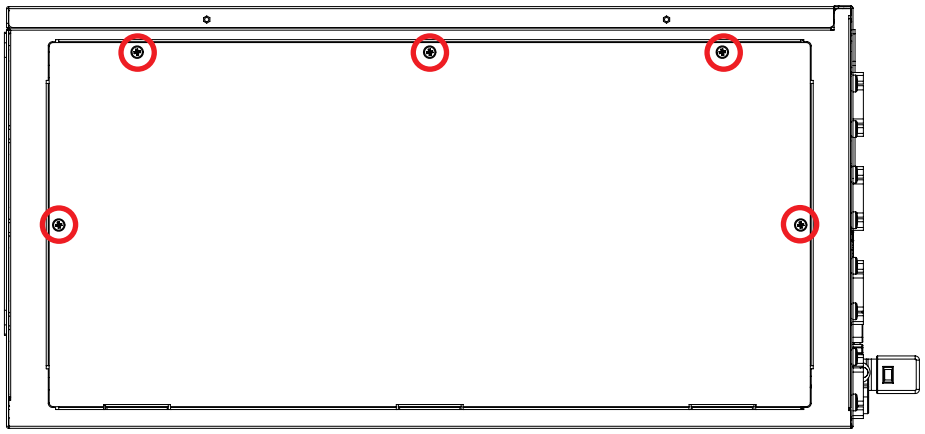


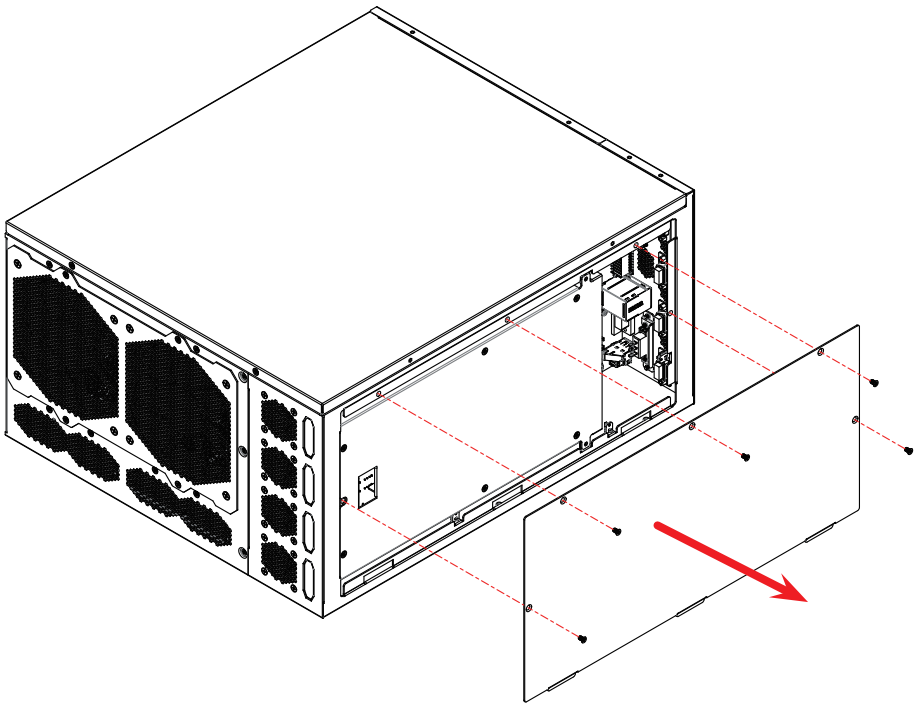
Step 4 Lock the U.2 tray with the key.



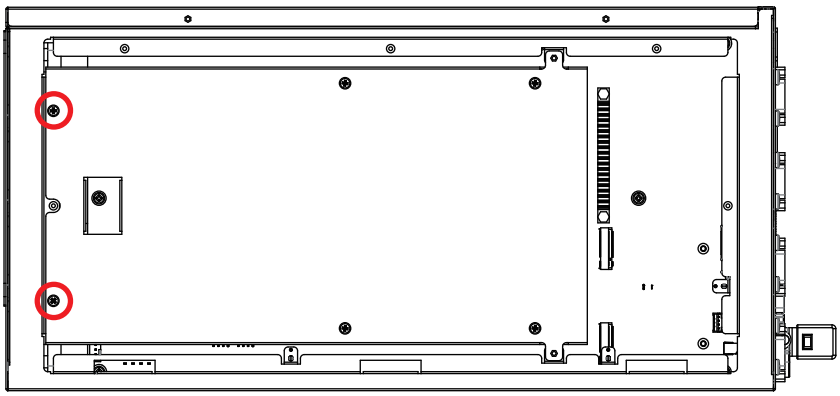
3.6 Installing M.2

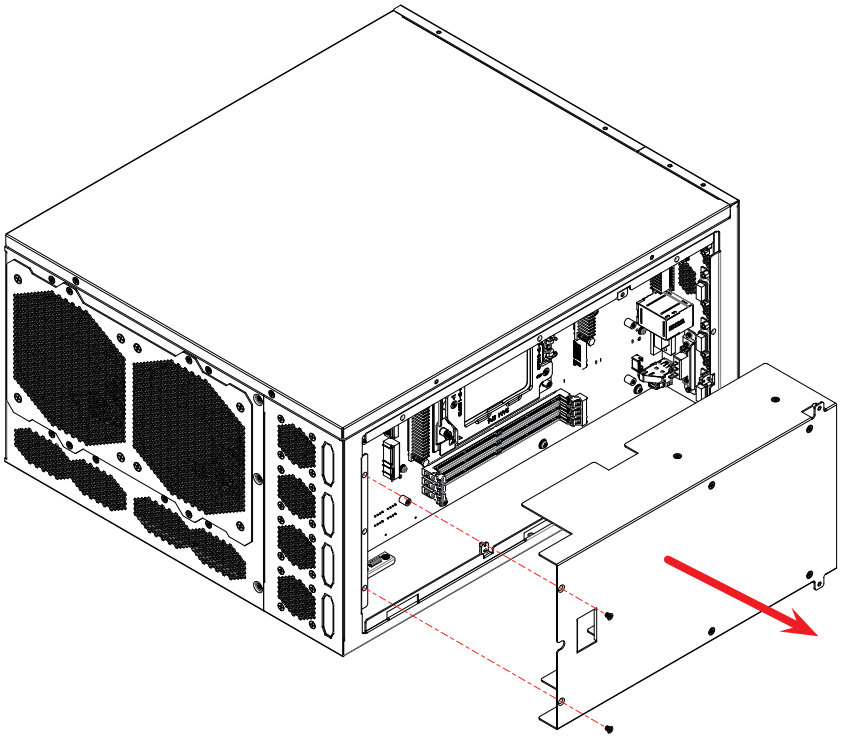
Step 1 Remove five flat head M3x5L screws and side cover.



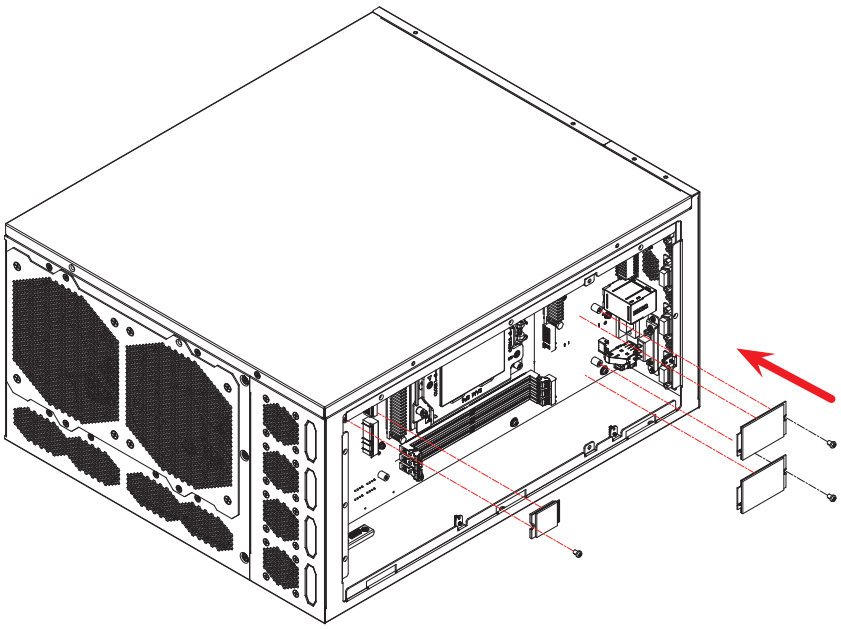


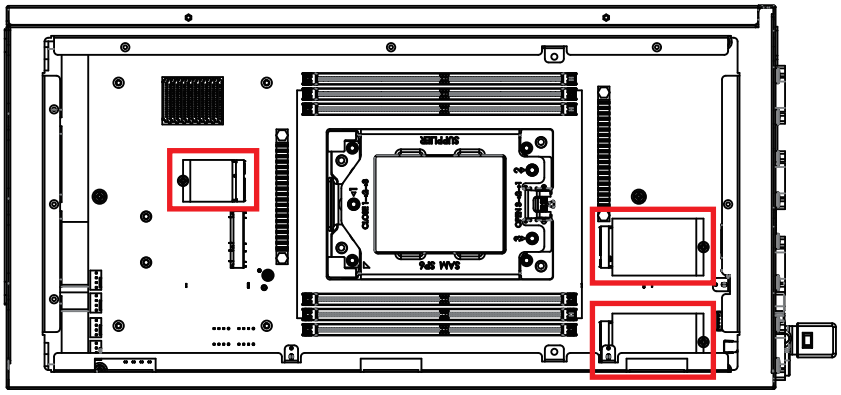
Step 2 Remove two flat head M3x5L screws and air duct.





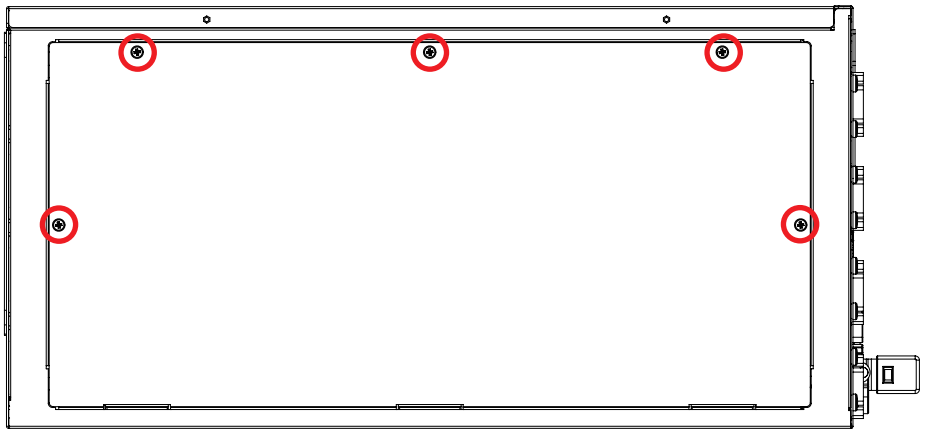
Step 3 Install three P head M3x4L screws and M.2 card.

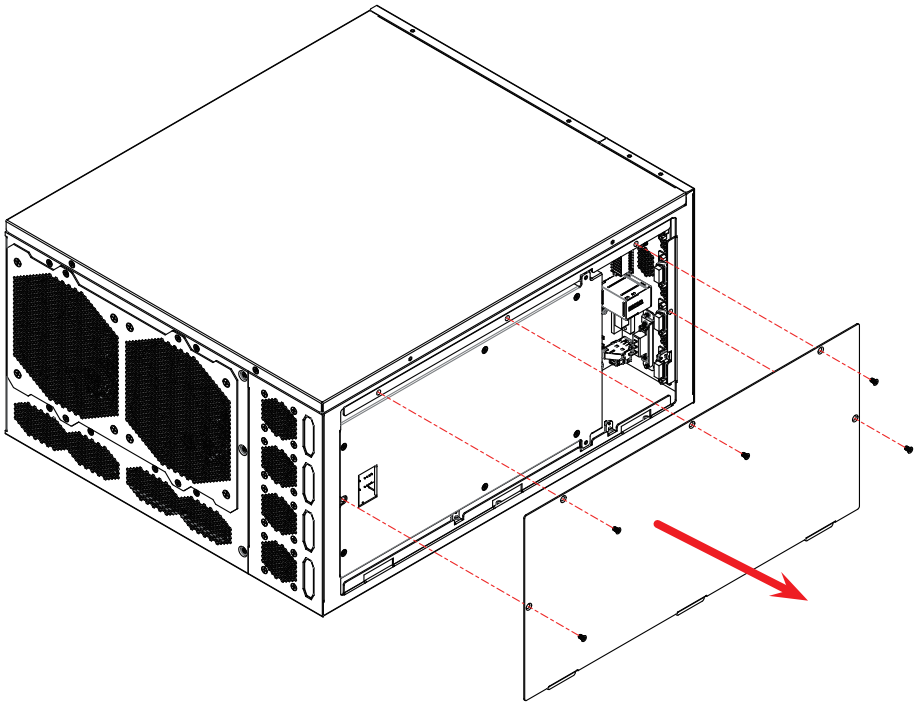




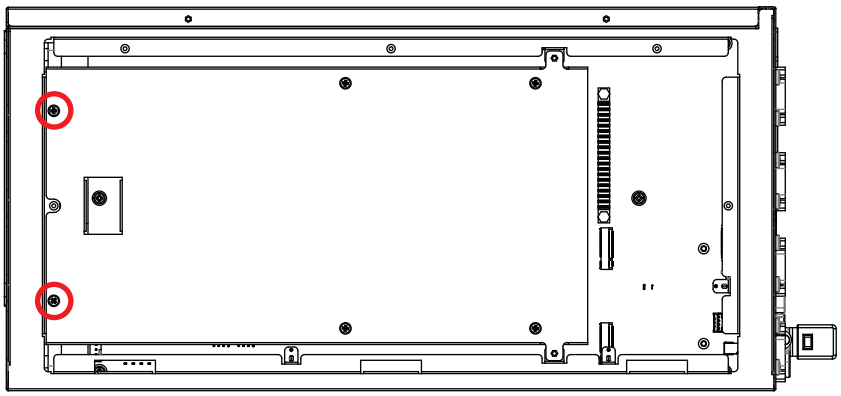
3.7 Installing Mini Pcie card

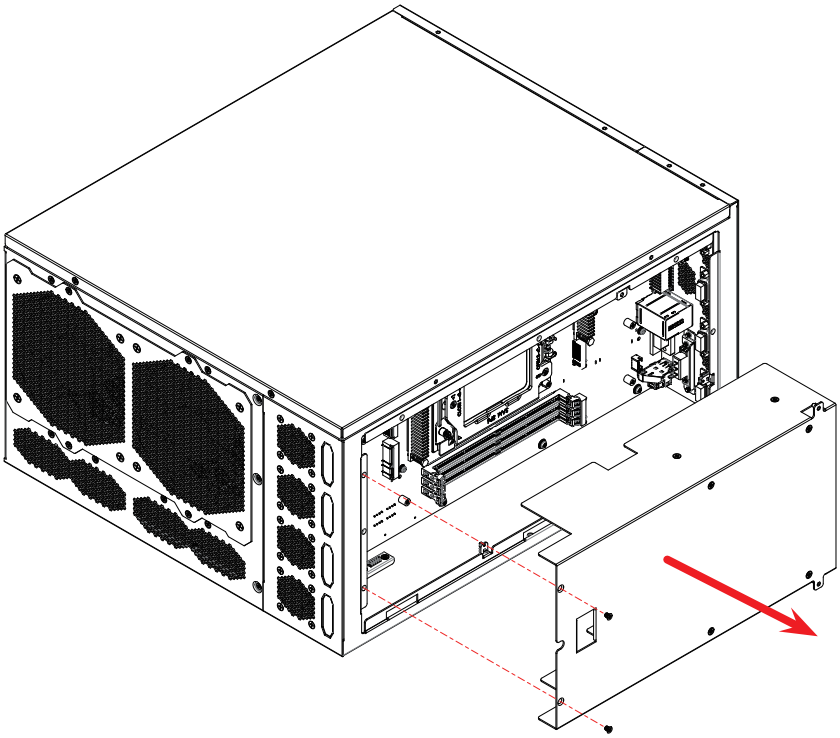
Step 1 Remove five flat head M3x5L screws and side cover.



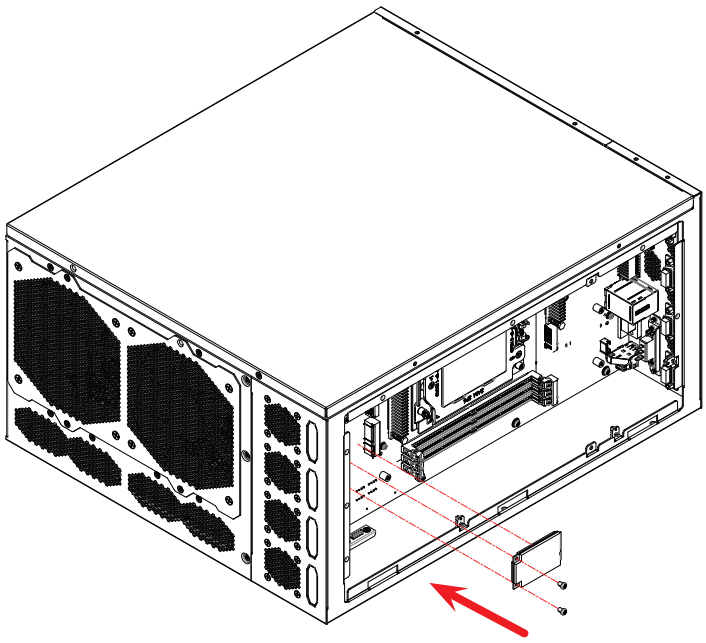


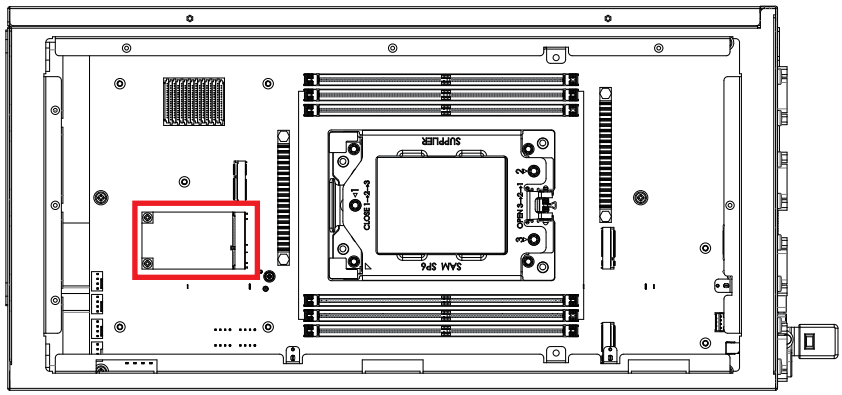
Step 2 Remove two flat head M3x5L screws and air duct.





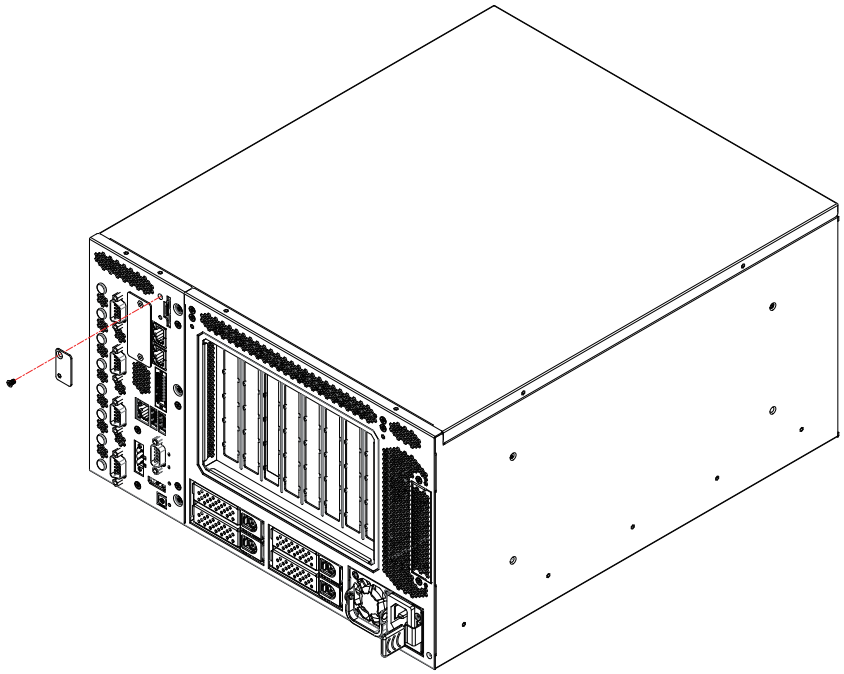
Step 3 Install two P head M3x4L screws and mini Pcie card.



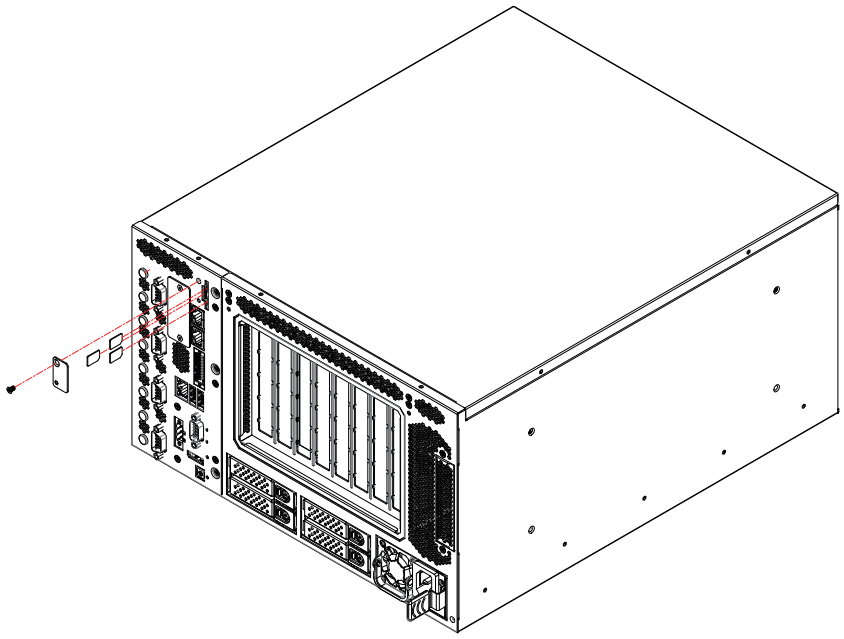


3.8 Installing SIM Card

Step 1 Remove flat head M3x5L screws and SIM cover.

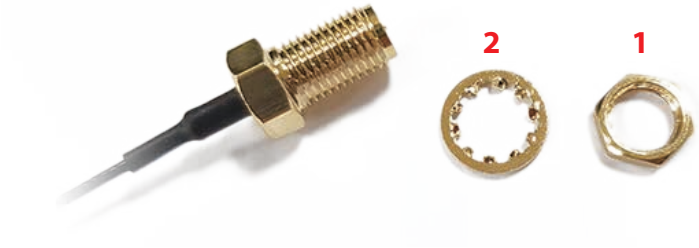


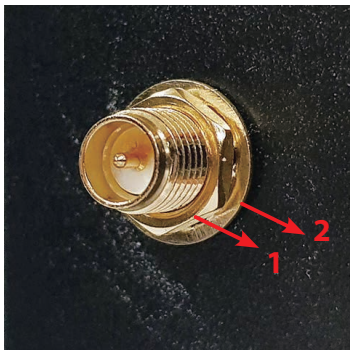
Step 2 Install SIM card and SIM cover with flat head M3x5L screws.



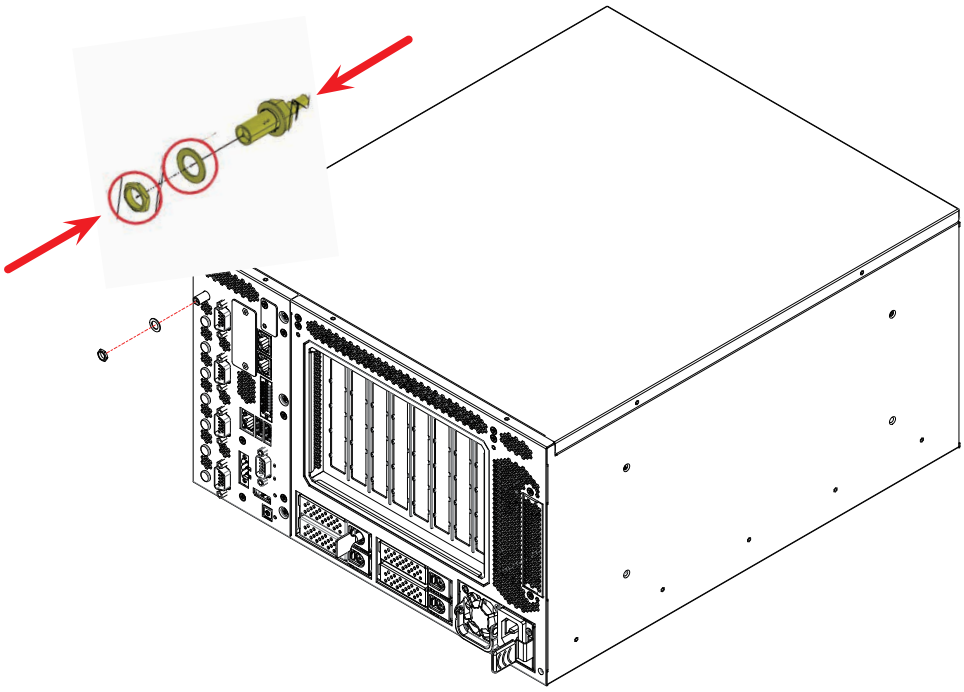
3.9 Installing Antenna Cable

Step 1 Check antenna parts (cable and washers).



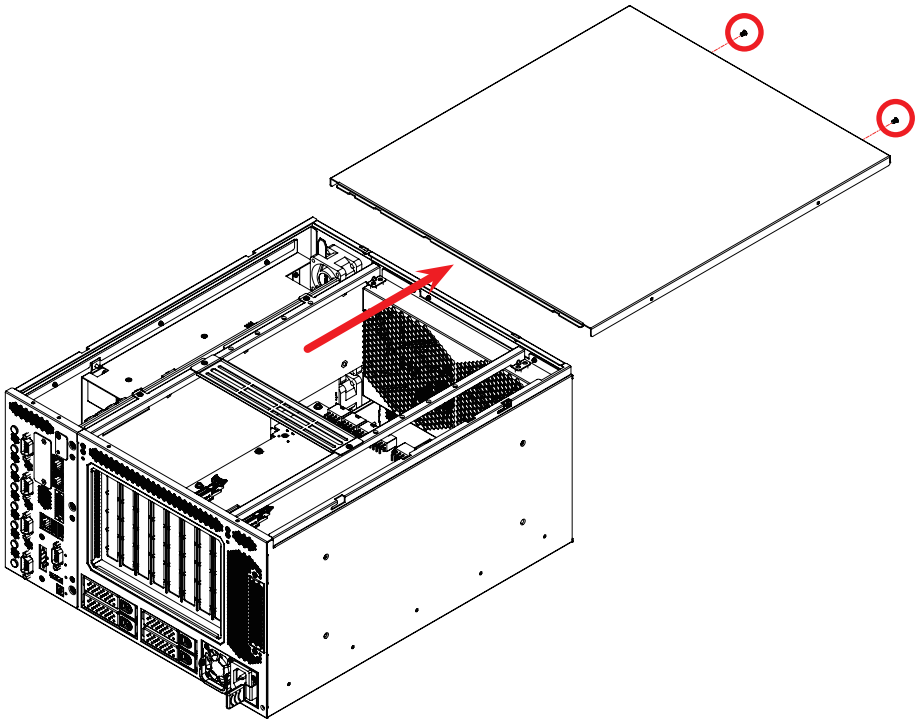


Step 2 Install the antenna.

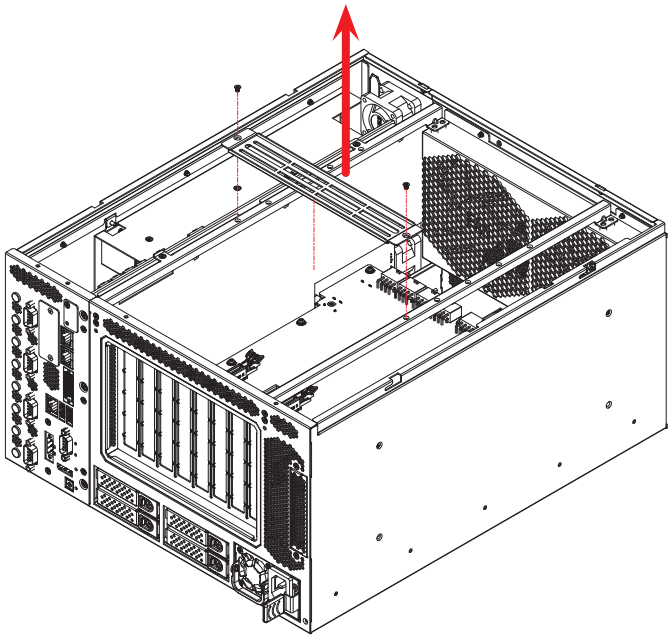


3.10 Installing Hold-down Kit

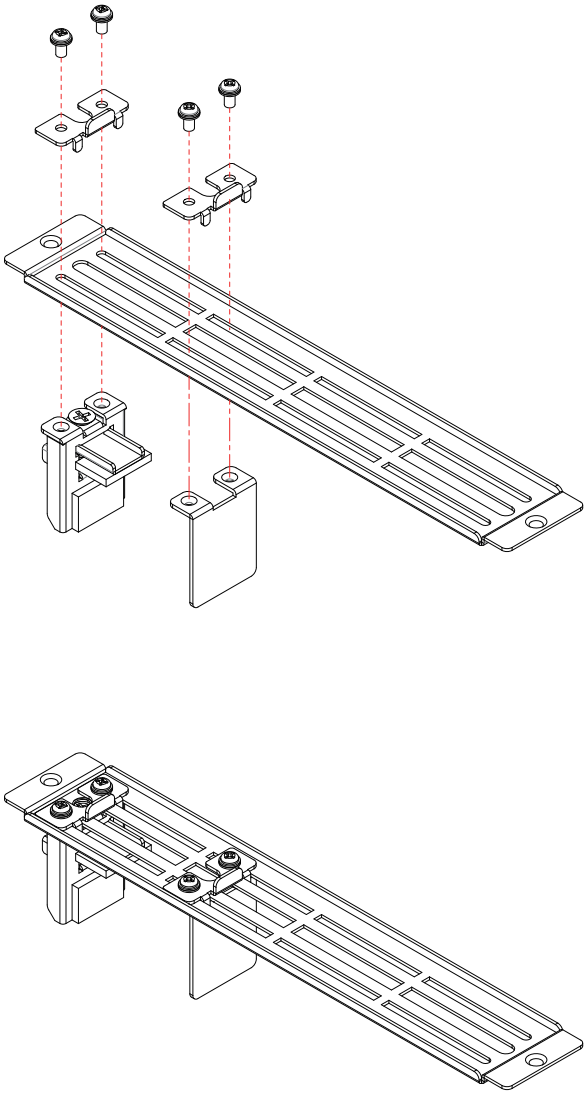
Step 1 Loosen the two M3 x 4L screws with F heads and adjust them to the desired clamping



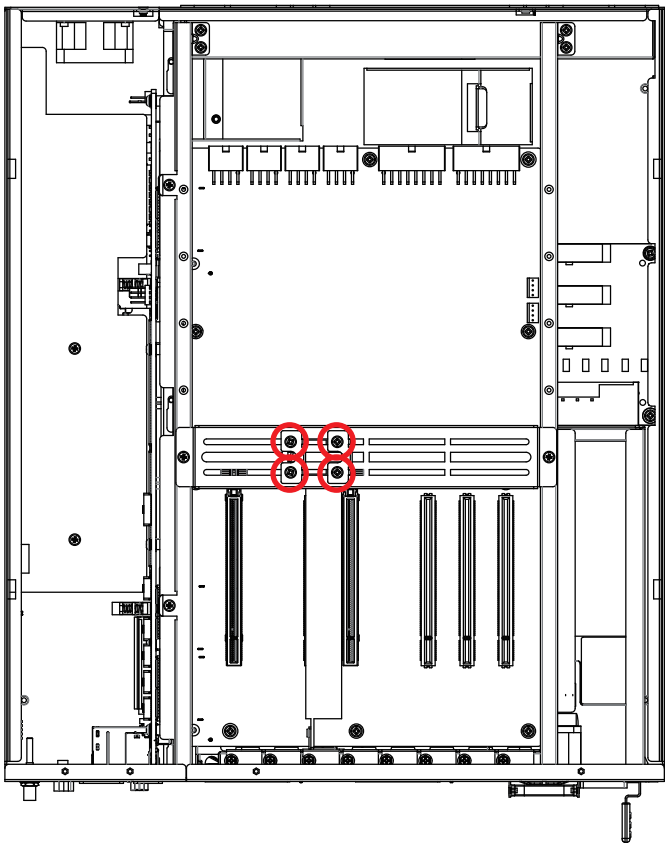
Step 2 Remove two flat head M3x4L screws.



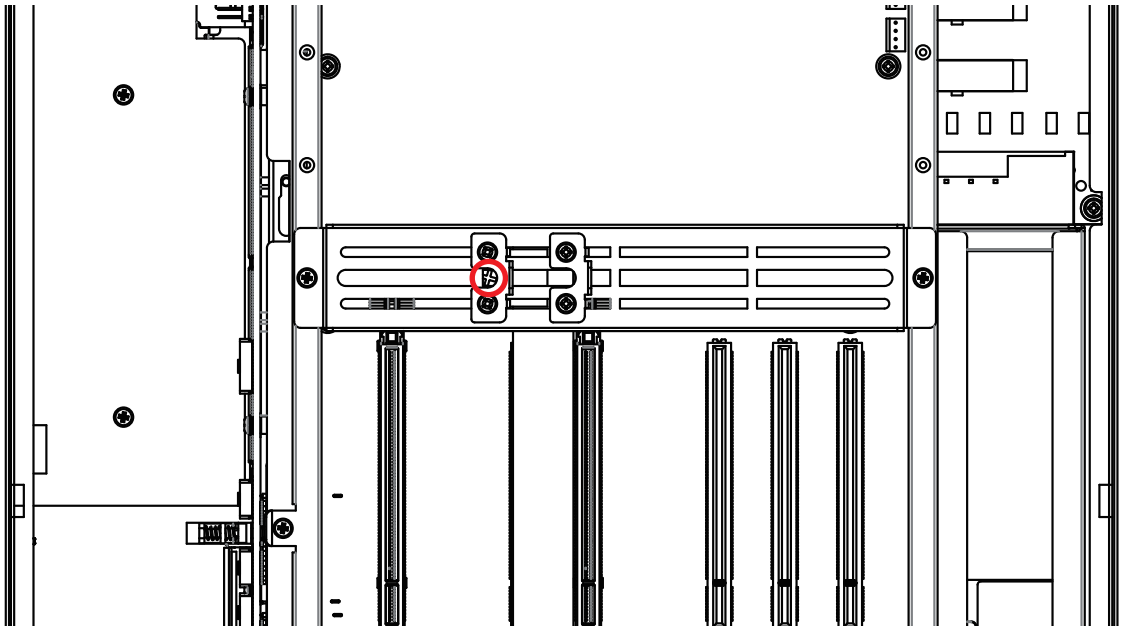
Step 3 Assemble the GPU Holder and Slide-rail using P head M3x4L screws.

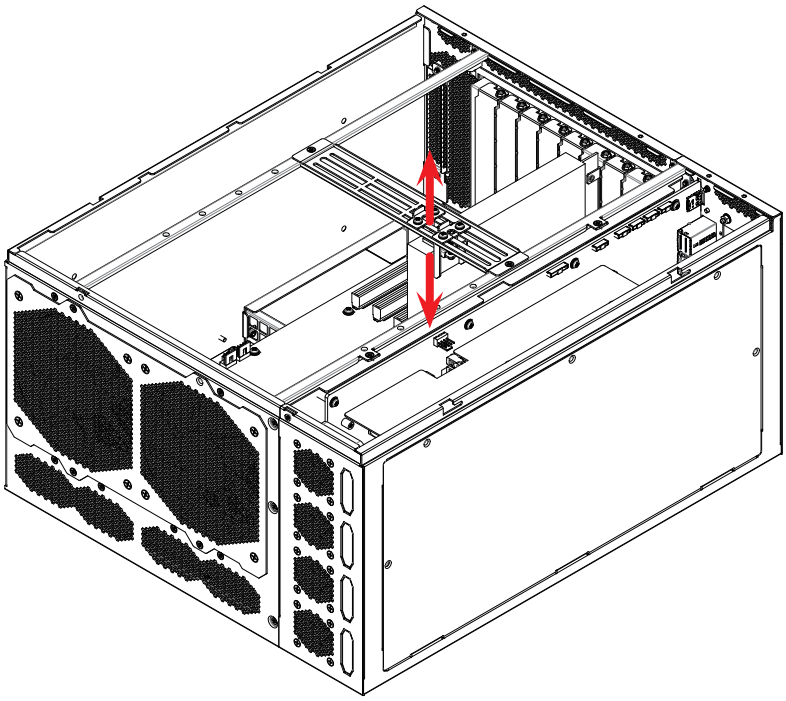


Step 4 After installing the card, adjust the left and right spacers to secure the card to the bracket, then tighten the four screws.



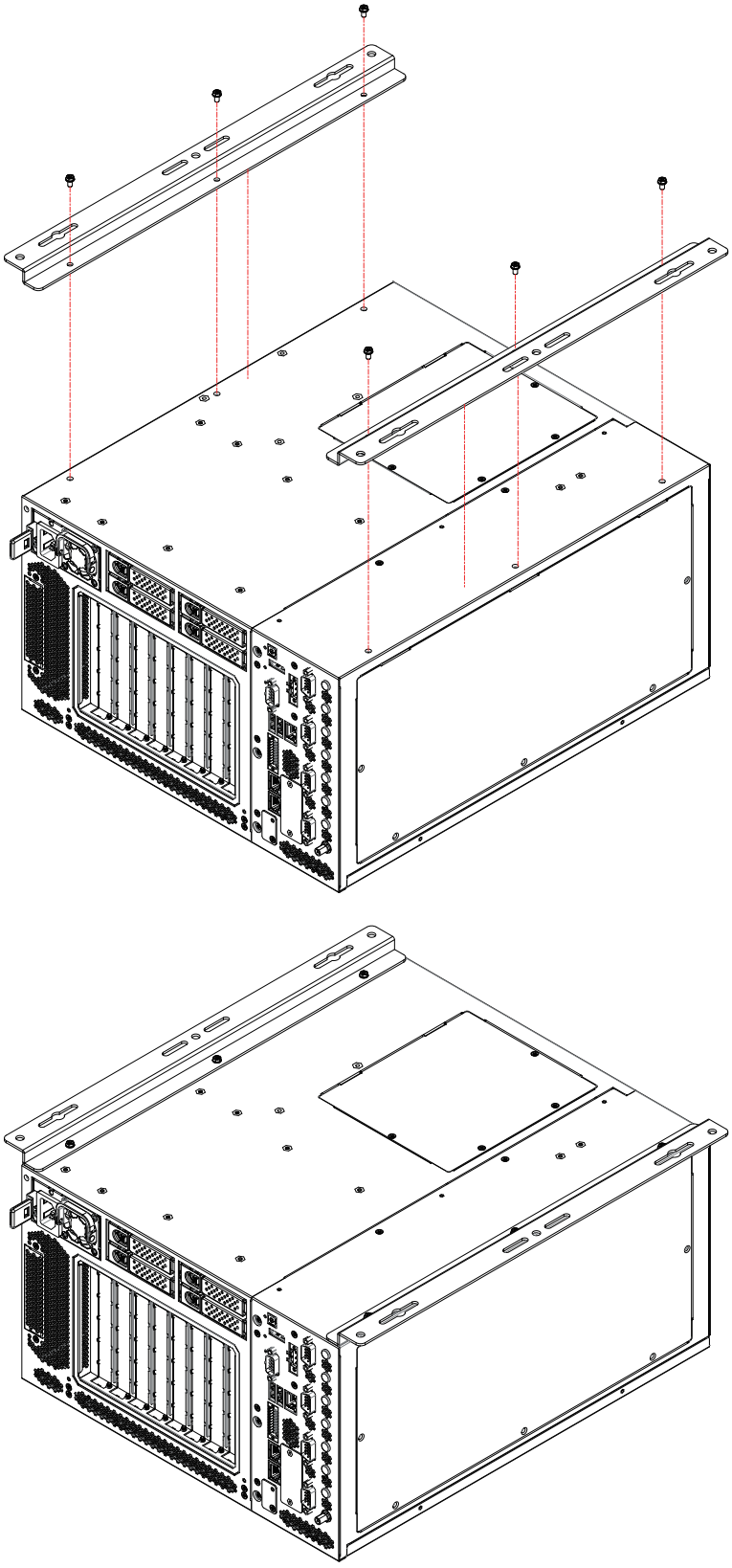
Step 5 Turn the screw (circle in red) left or right with Phillips screwdriver to adjust the pad up and down.





3.11 Mounting Your ICS-2000

Install the wall mount bracket and using P head M4x6L screws.



4

BIOS SETUP

4.1 BIOS Settings

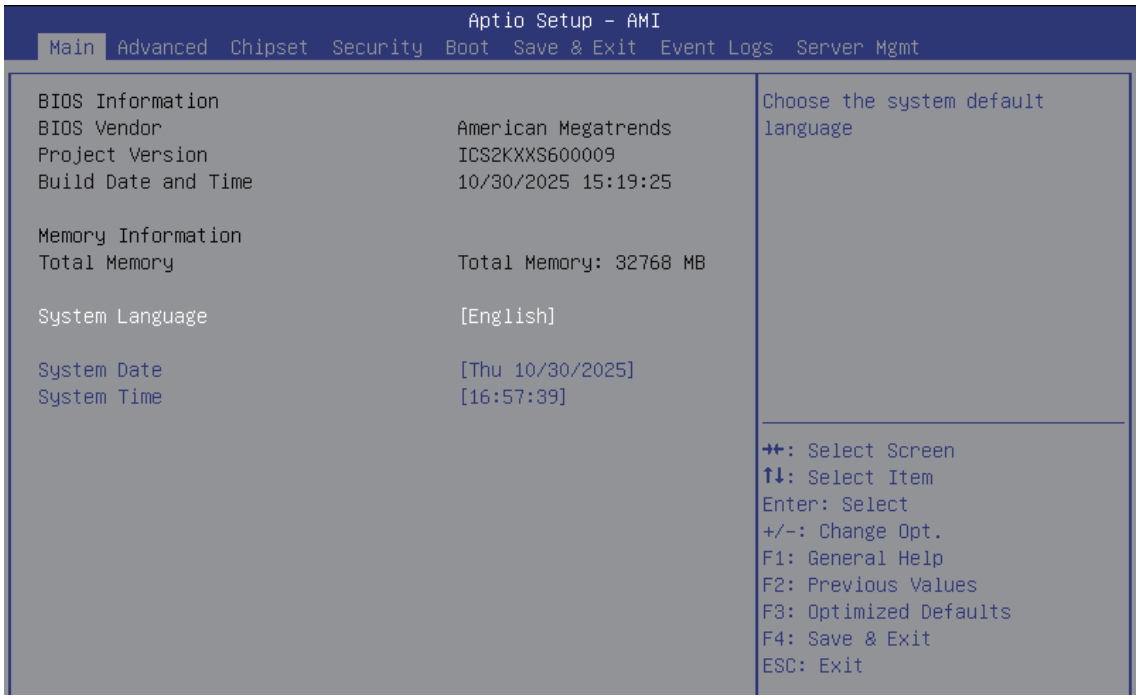


Figure 4-1 : Entering Setup Screen

BIOS provides an interface for users to check and change system configuration. The BIOS setup program is accessed by pressing the <Del> key when POST display output is shown.

4.2 Main Menu

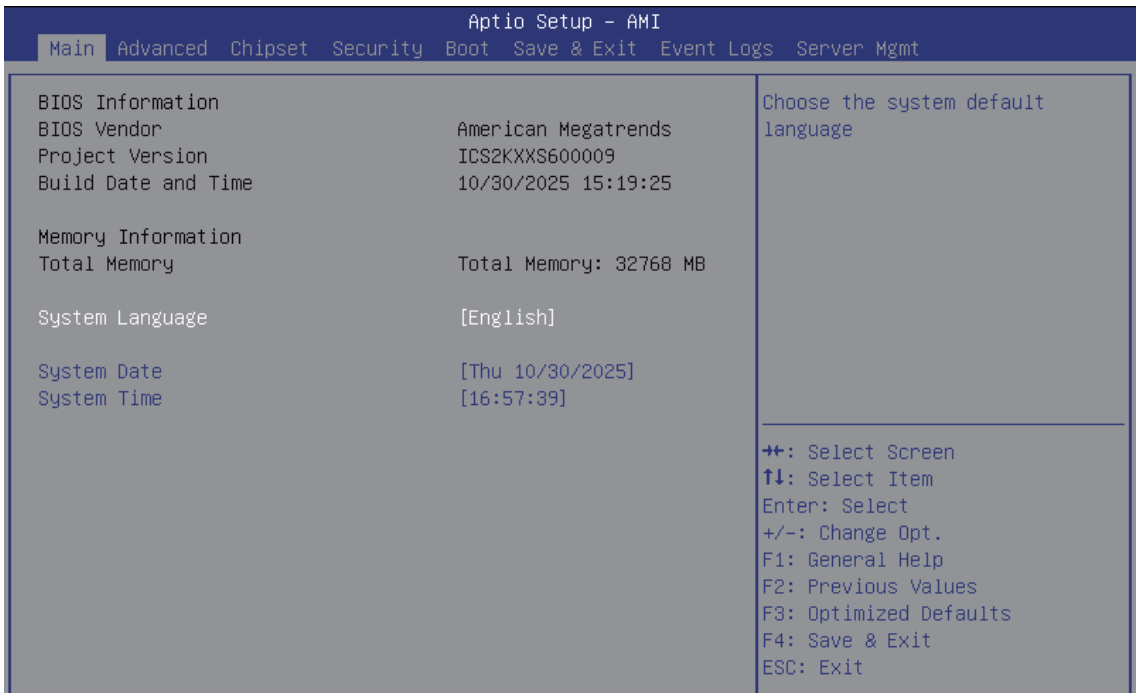


Figure 4-2 : BIOS Main Menu

The main menu displays BIOS version and system information. There are two options on Main menu.

System Date

Set the Date. Use <Tab> to switch between Date elements.
Default Ranges:
Year: 1998-9999
Months: 1-12
Days: Dependent on month
Range of Years may vary.

System Time

Set the Time. Use <Tab> to switch between Time elements.

4.3 Advanced Menu

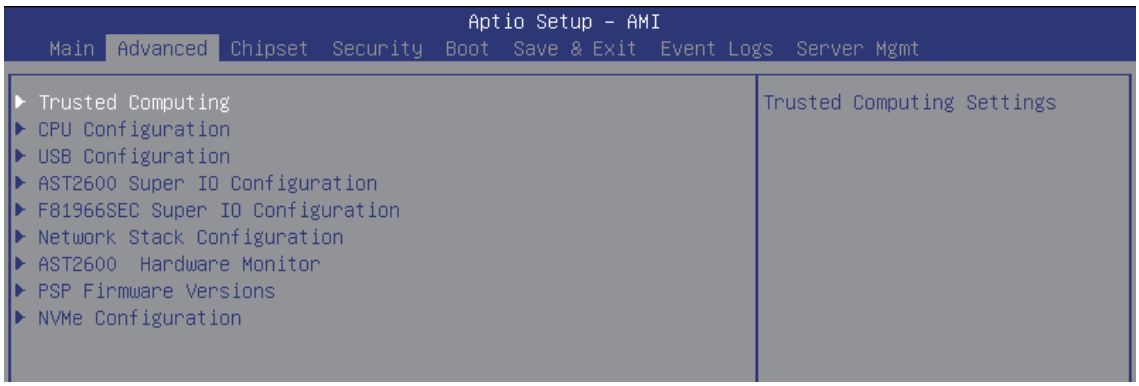


Figure 4-3 : BIOS Advanced Menu

Select advanced tab to enter advanced BIOS setup options, such as CPU configuration, ACPI settings, and Super IO configuration.

4.3.1 Trusted Computing

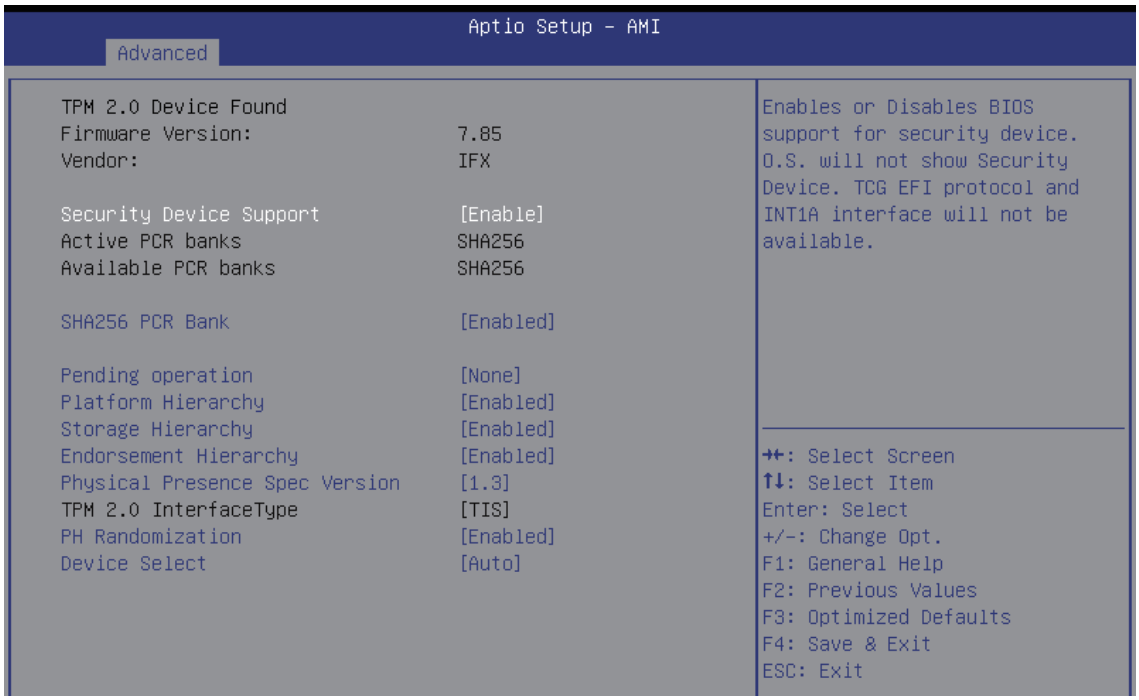


Figure 4-3-1 : Trusted Computing

Control the TPM device status and display related information if TPM chip is present.

4.3.2 CPU Configuration

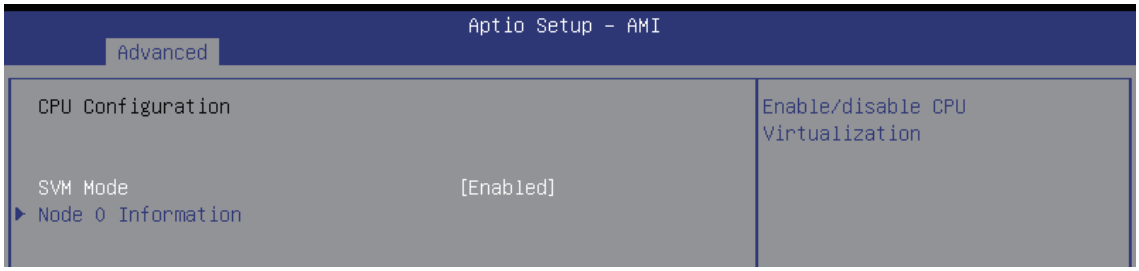


Figure 4-3-2 : CPU Configuration

SVM Mode

Enable/disable CPU Virtualization.

4.3.2.1 Node 0 Information

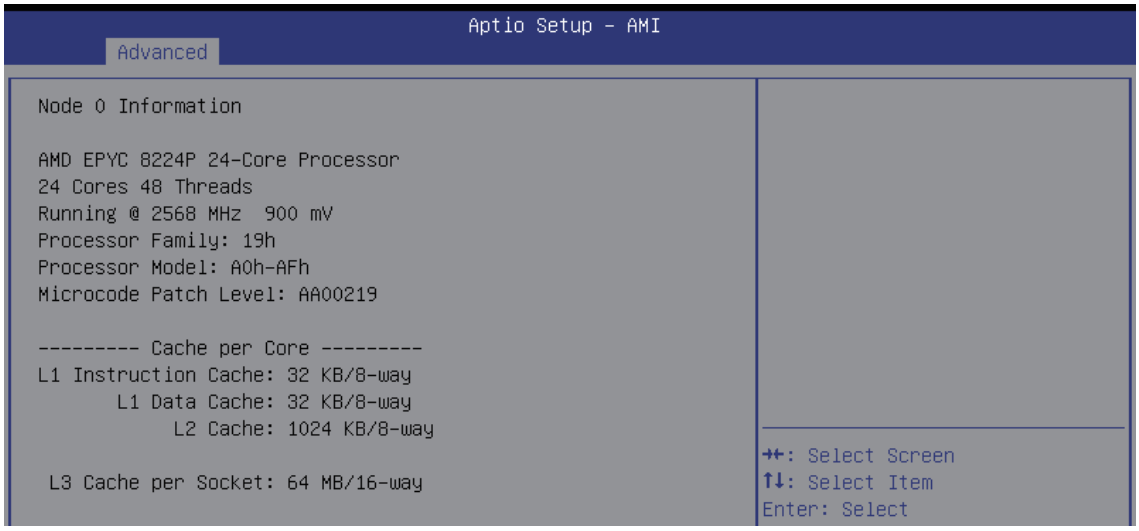


Figure 4-3-2-1 : Node 0 Information

View Memory Information related to Node 0.

4.3.3 USB Configuration

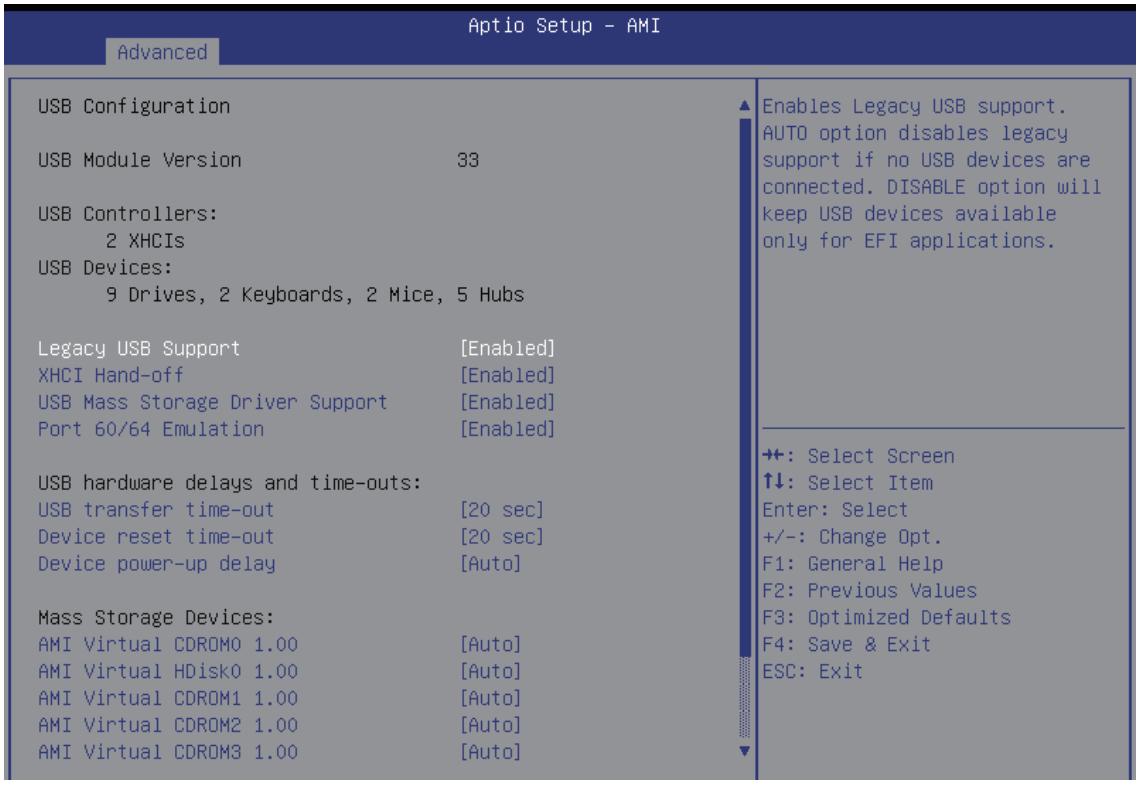


Figure 4-3-3 : USB Configuration

Legacy USB Support

Enables Legacy USB support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

USB Mass Storage Driver Support

Enable/Disable USB Mass Storage Driver Support.

Port 60/64 Emulation

Enables I/O port 60h/64h emulation support.

USB transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

Device reset time-out

USB mass storage device Start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

4.3.4 AST2600 Super IO Configuration



Figure 4-3-4 : AST2600 Super IO Configuration

Control AST2600 Serial Port Configuration.

4.3.4.1 AST2600 Serial Port 1 Configuration

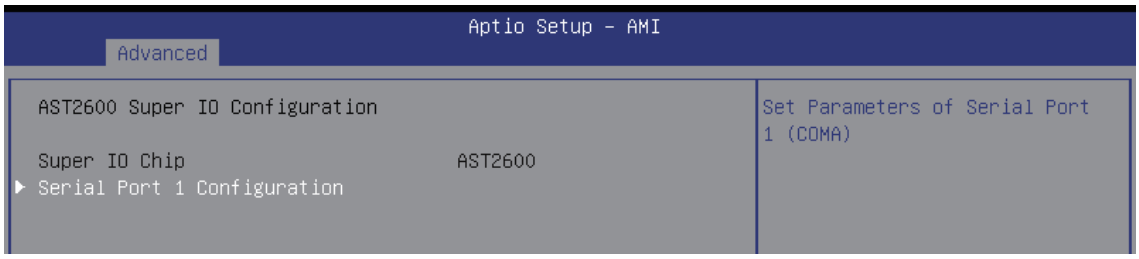


Figure 4-3-4-1 : AST2600 Serial Port 1 Configuration

Serial Port

Enable or Disable AST2600 Serial Port 1 (COM5).

Change Settings

Select AST2600 serial port I/O resource.

4.3.5 F81966SEC Super IO Configuration



Figure 4-3-5 : F81966SEC Super IO Configuration

4.3.5.1 Serial Port X Configuration

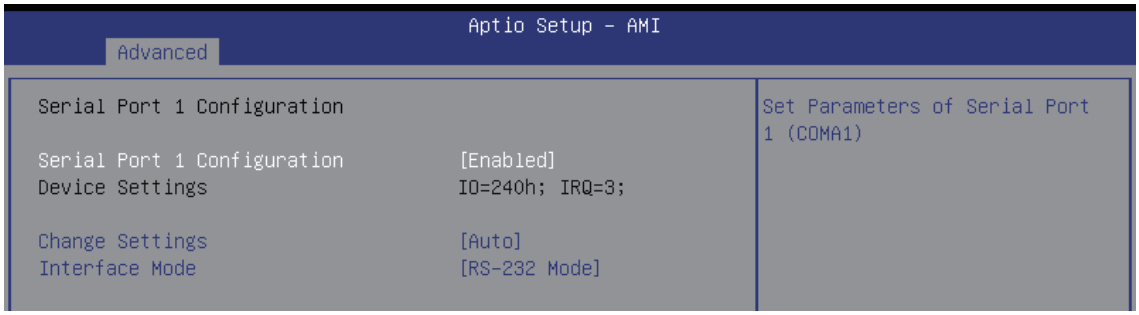


Figure 4-3-5-1 : Serial Port X Configuration

Serial Port
Enable or Disable F81966SEC Serial Port1-4 (COM1-4)
Change Settings
Select F81966SEC serial port1-4 I/O resource.
Interface Mode
Select Device Mode.

4.3.6 Network Stack Configuration

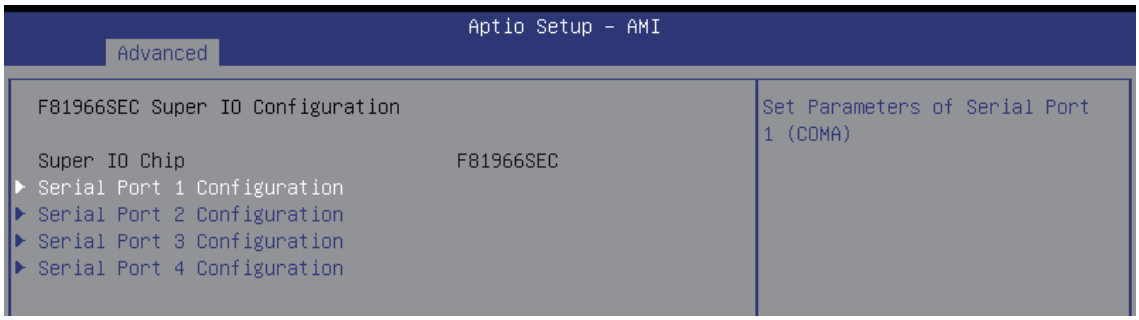


Figure 4-3-6 : Network Stack Configuration

Network Stack
Enable/Disable UEFI Network Stack
IPv4 PXE Support
Enable/Disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
IPv4 HTTP Support
Enable/Disable IPv4 HTTP boot support. If disabled, IPv4 HTTP boot support will not be available.
IPv6 PXE Support
Enable/Disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.
IPv6 PXE Support
Enable/Disable IPv6 HTTP boot support. If disabled, IPv6 HTTP boot support will not be available.
PXE boot wait time
Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.
Media detect count
Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

4.3.7 AST2600 Hardware Monitor

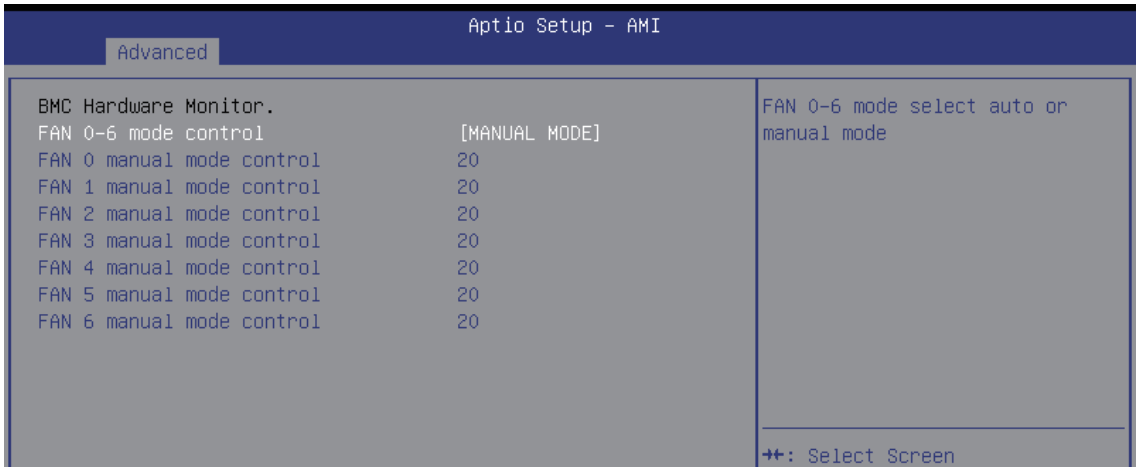


Figure 4-3-7 : AST2600 Hardware Monitor

Control BMC hardware monitor fan speed auto or manual mode configuration.

4.3.8 PSP Firmware Versions

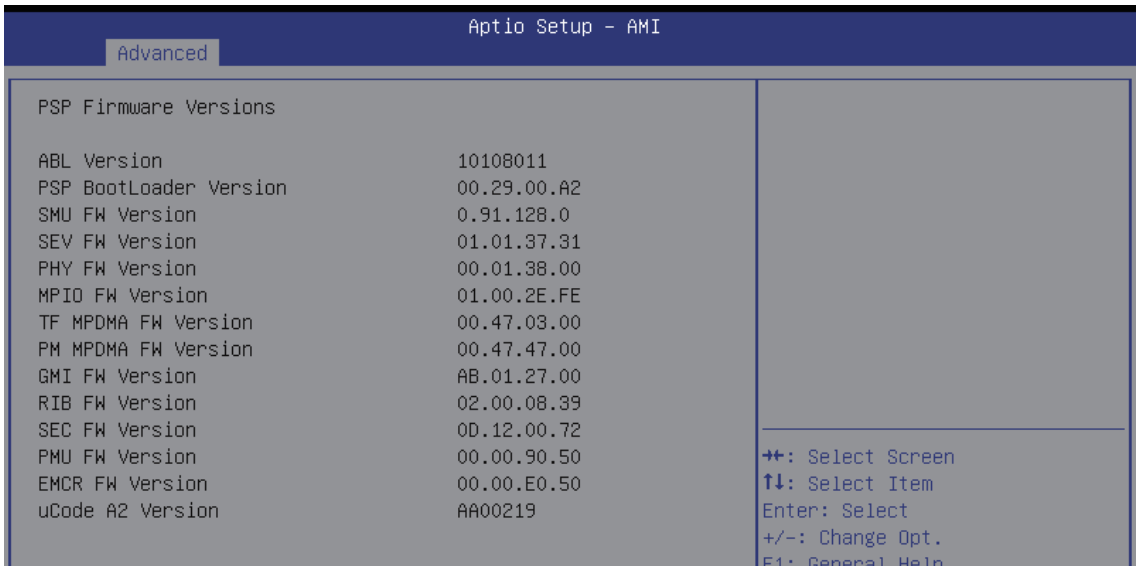


Figure 4-3-8 : PSP Firmware Versions

Display PSP firmware versions information.

4.3.9 NVMe Configuration



Figure 4-3-9 : NVMe Configuration

Display NVMe controller and Drive information.

4.4 Chipset Menu

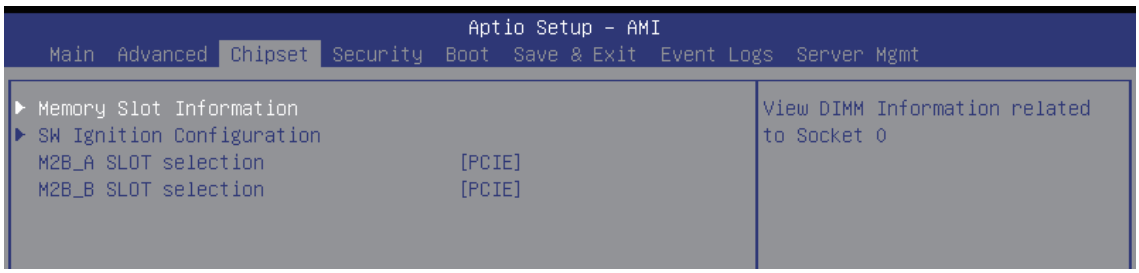


Figure 4-4 : BIOS Chipset Menu

Select Chipset tab to enter chipset BIOS setup options, such as Memory Slot Information, and SW Ignition Configuration.

M2B_A SLOT selection
M2B_A SLOT selection PCIE or USB3.0.
M2B_B SLOT selection
M2B_A SLOT selection PCIE or USB3.0.

4.4.1 Memory Slot Information

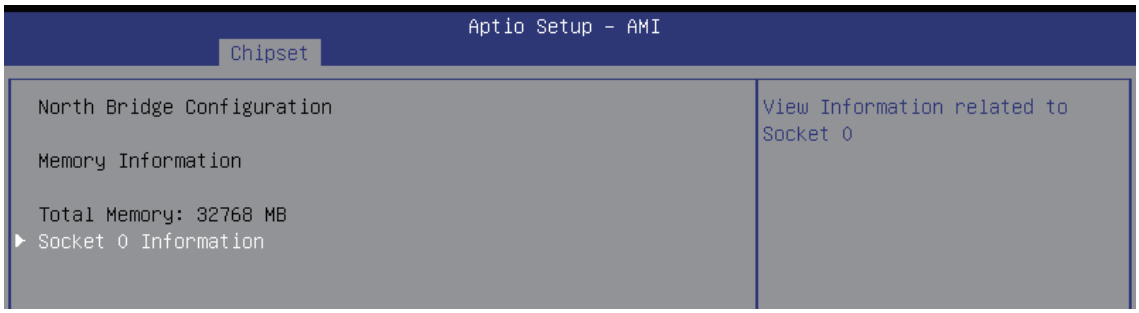


Figure 4-4-1 : Memory Slot Information

4.4.1.1 Socket 0 Information

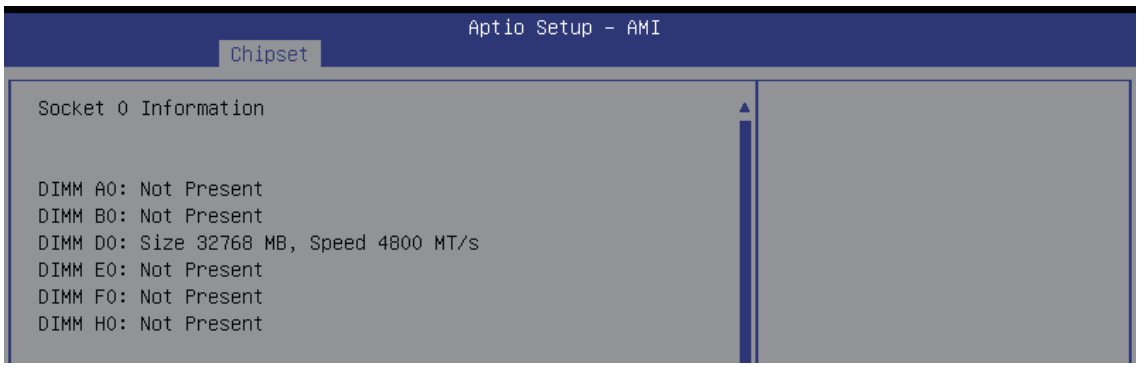


Figure 4-4-1-1 : Socket 0 Information

Displays memory information.

4.4.2 SW Ignition Configuration

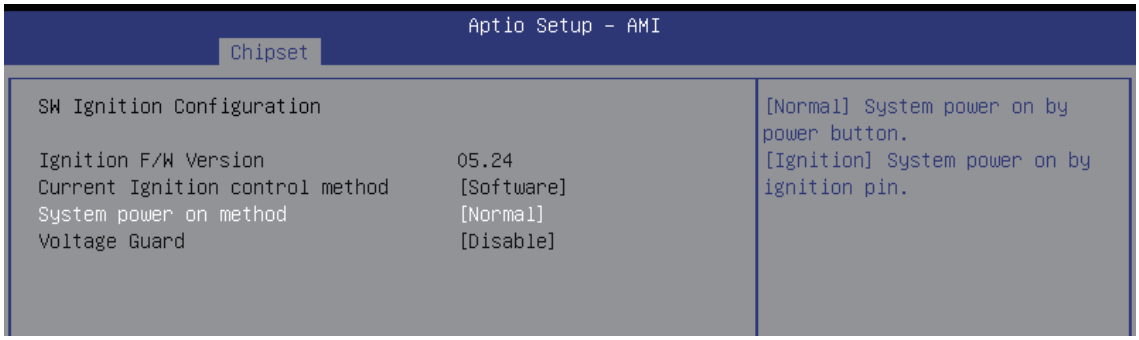


Figure 4-4-2 : SW Ignition Configuration

System power on method

[Normal] System power on by power button.
[Ignition] System power on by ignition pin.

Delay On Timer (Seconds)

The delay time after user trigger ignition on signal (Seconds).

Delay Off Timer (Seconds)

The delay time after user trigger ignition off signal (Seconds).

Force Shutdown Timer (Minutes)

Used to force cut off system power when OS unable gracefully shutdown system successfully.

4.5 Security Menu

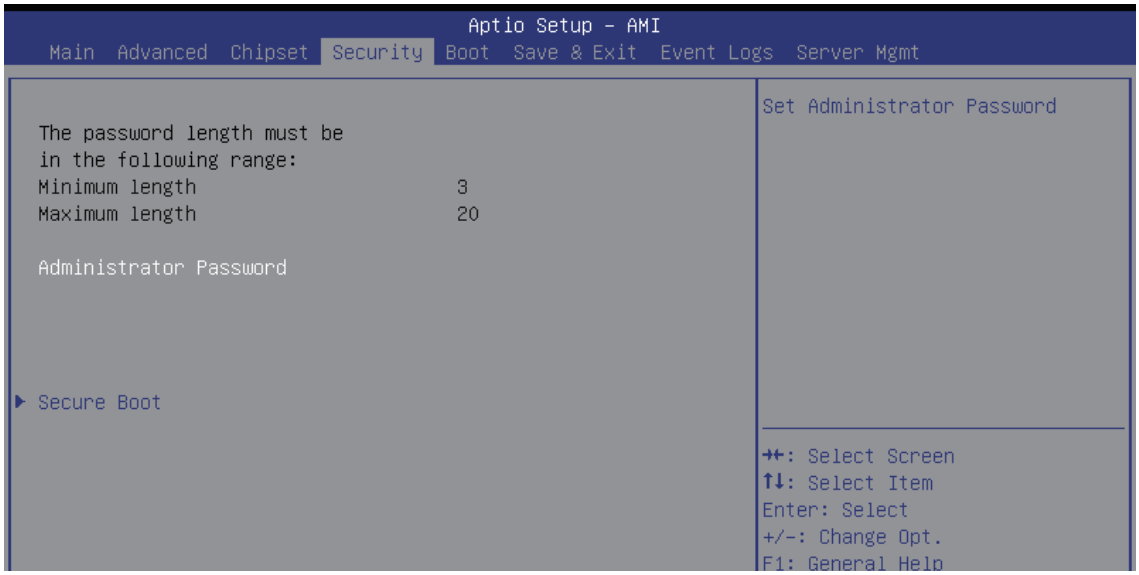


Figure 4-5 : BIOS Security Menu

Administrator Password

Set administrator password.

4.5.1 Secure Boot



Figure 4-5-1 : Secure Boot

Secure Boot

Secure Boot feature is Active if Secure Boot is Enabled, Platform Key(PK) is enrolled and the System is in User mode. The mode change requires platform reset.

Secure Boot Mode

Secure Boot mode options: Standard or Custom.

In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.

Restore Factory Keys

Force System to User Mode. Install factory default Secure Boot key databases.

Reset To Setup Mode

Delete all Secure Boot key databases from NVRAM.

Key Management

Enables expert users to modify Secure Boot Policy variables without variable authentication.

4.6 Boot Menu

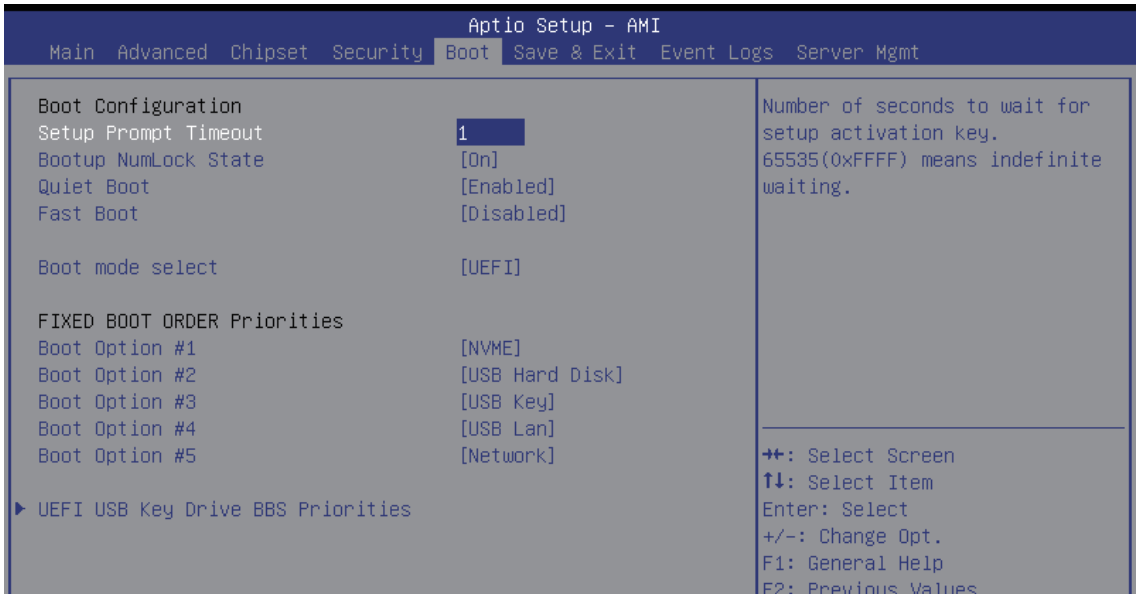


Figure 4-6 : BIOS Boot Menu

Setup Prompt Timeout

Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

Enables or disables Quiet Boot option.

Fast Boot

Enables or disables boot with initialization of a minimal set of devices required to launch active boot option.

Boot mode select

boot mode only support UEFI.

Boot Option Priorities

Sets the system boot order.

4.7 Save & Exit

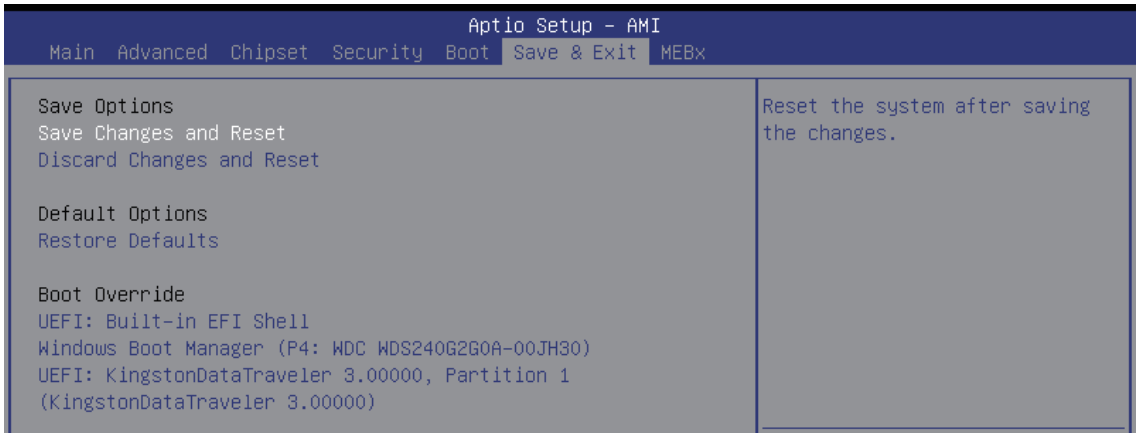


Figure 4-7 : BIOS Save & Exit Menu

Save Changes and Reset

Reset the system after saving the changes.

Discard Changes and Reset

Reset system setup without saving any changes.

Restore Defaults

Restore/Load Default values for all the setup options.

4.8 Event Logs

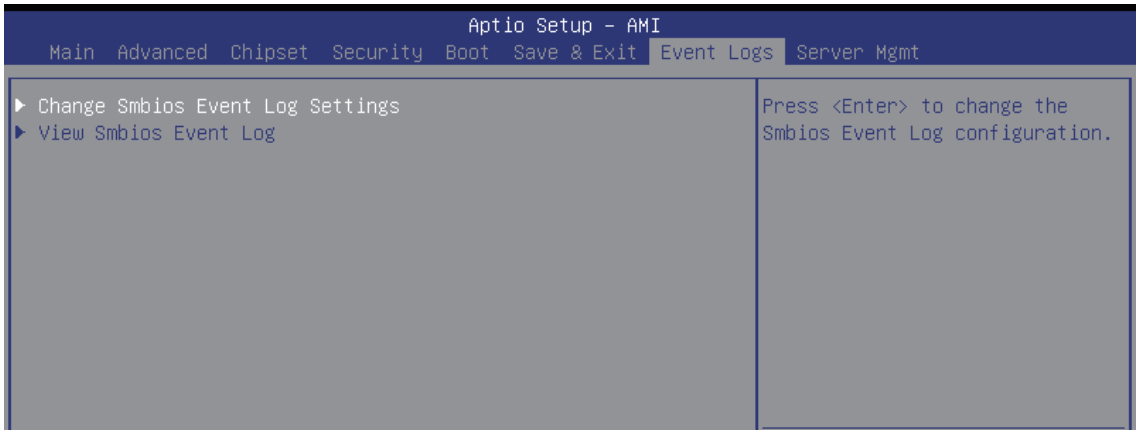


Figure 4-8 : Event Logs

Change Smbios Event Log Setting

Change the Smbios Event Log configuration.

View Smbios Event Log

View the Smbios Event Log records.

4.8.1 Change Smbios Event Log Setting

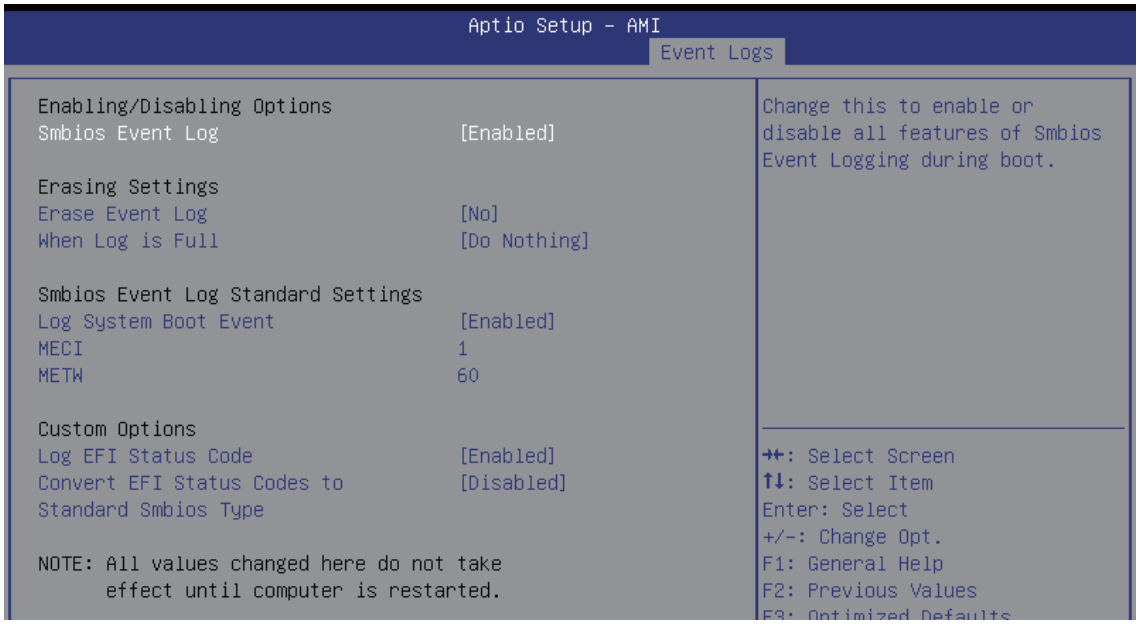


Figure 4-8-1 : Change Smbios Event Log Setting

Smbios Event Log
Change this to enable or disable all features of Smbios Event Logging during boot.
View Smbios Event Log
View the Smbios Event Log records.
Smbios Event Log
Choose options for erasing Smbios Event Log.
When Log is Full
Choose options for reactions to a full Smbios Event Log.
Log System Boot Event
Choose option to enable/disable logging of System boot event.
MECI
Mutiple Event Count Increment.
METW
Mutiple Event Time Window.
Log EFI Status Code
Enable or disable the logging of EFI Status Codes as OEM reserved type E0.
Convert EFI Status Codes to Standard Smbios Type
Enable or disable the converting of EFI Status Codes to Standard Smbios Types.

4.8.2 View Smbios Event Log

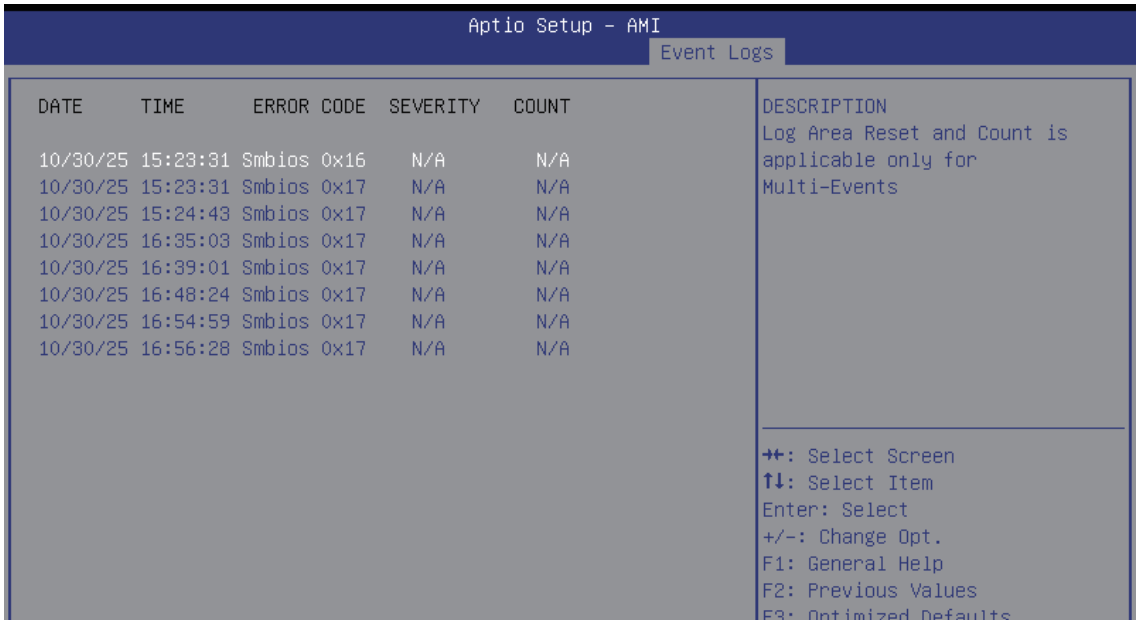


Figure 4-8-2 : View Smbios Event Log

View the Smbios Event Log records.

4.9 Server Mgmt

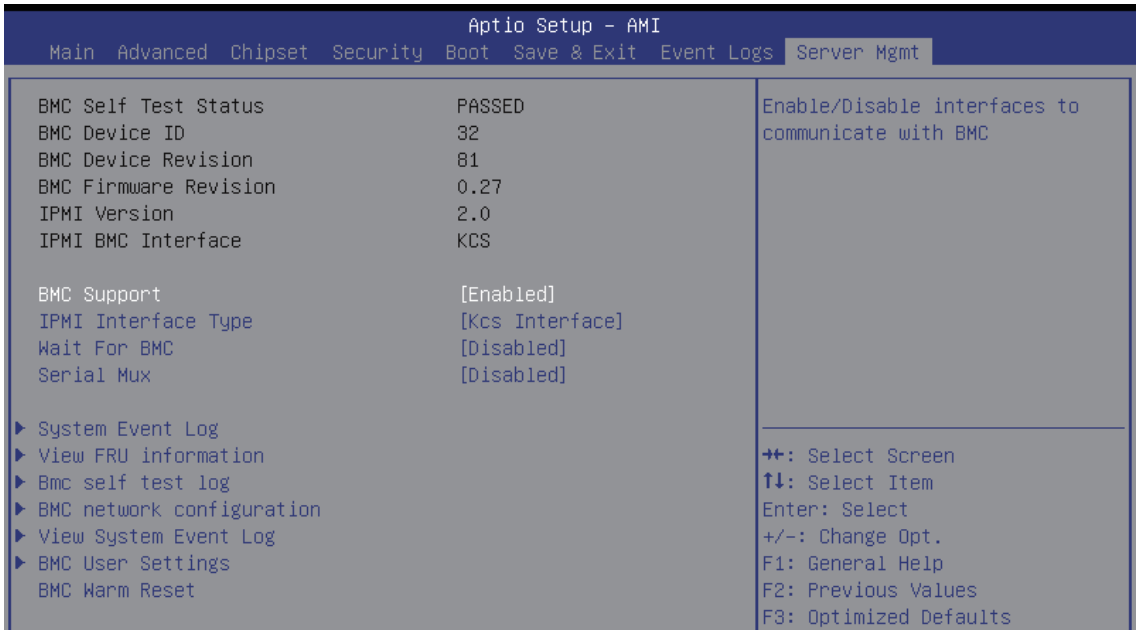


Figure 4-9 : Server Mgmt

BMC Support
Enable or Disable interfaces to communicate with BMC.

IPMI Interface Type
Type of Interface to communicate BMC from HOST.

Wait For BMC
Wait For BMC response for specified time out.

Serial Mux
Enable or disable Serial Mux configuration.

BMC Warm Reset
Do Warm Reset BMC.

4.9.1 System Event Log

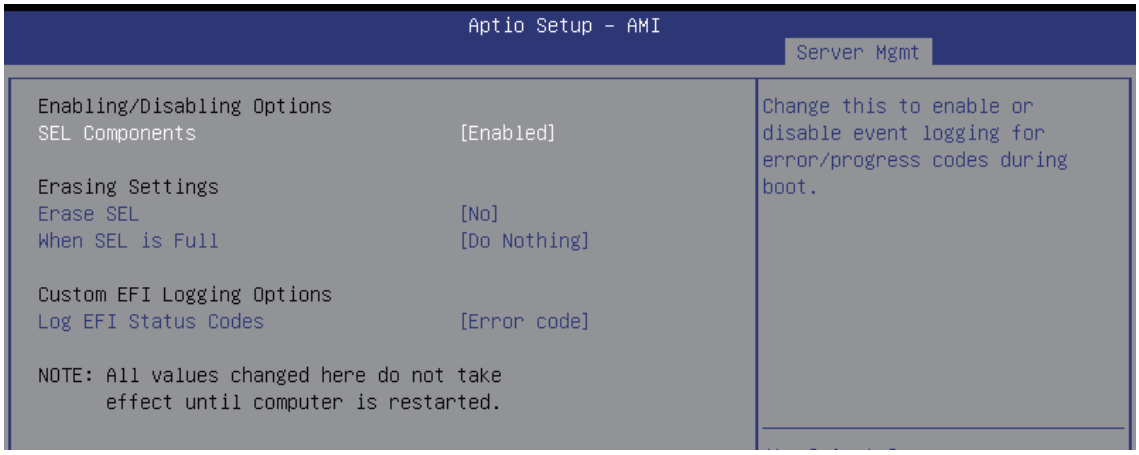


Figure 4-9-1 : System Event Log

SEL Components

Change this to enable or disable event logging for error progress codes during boot.

Erase SEL

Choose options for erasing SEL.

When SEL is Full

Choose options for reactions to a full SEL.

Log EFI Status Codes

Disable the logging of EFI Status Codes or log only error code or only progress code or both.

4.9.2 View FRU information

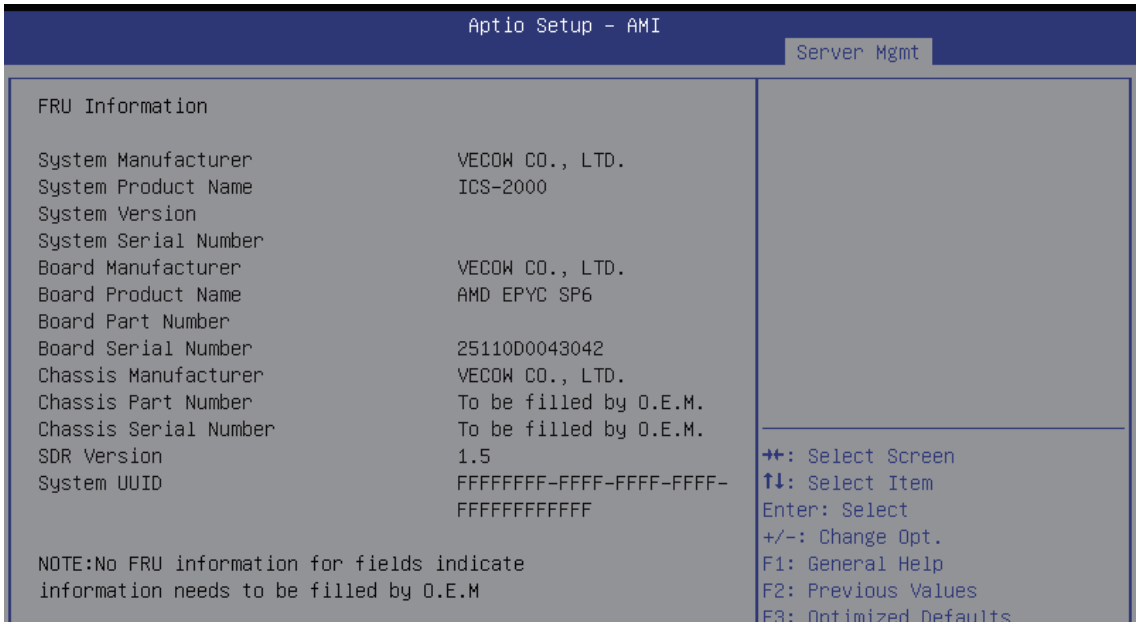


Figure 4-9-2 : View FRU information

View FRU information.

4.9.3 Bmc self test log



Figure 4-9-3 : Bmc self test log

Erase Log
Erase Log Options.
When log is full
Select the action to be taken when log is full.

4.9.4 BMC network configuration

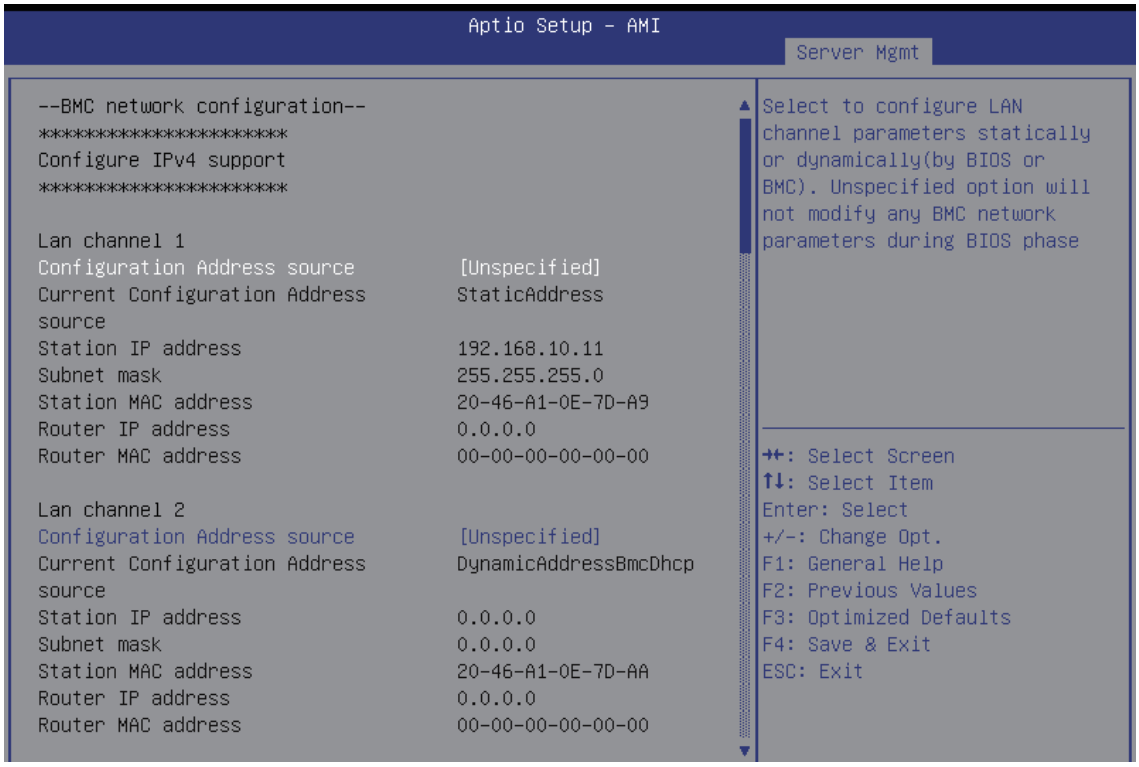


Figure 4-9-4 : BMC network configuration

BMC network IP&MAC address configuration.

4.9.5 View System Event Log

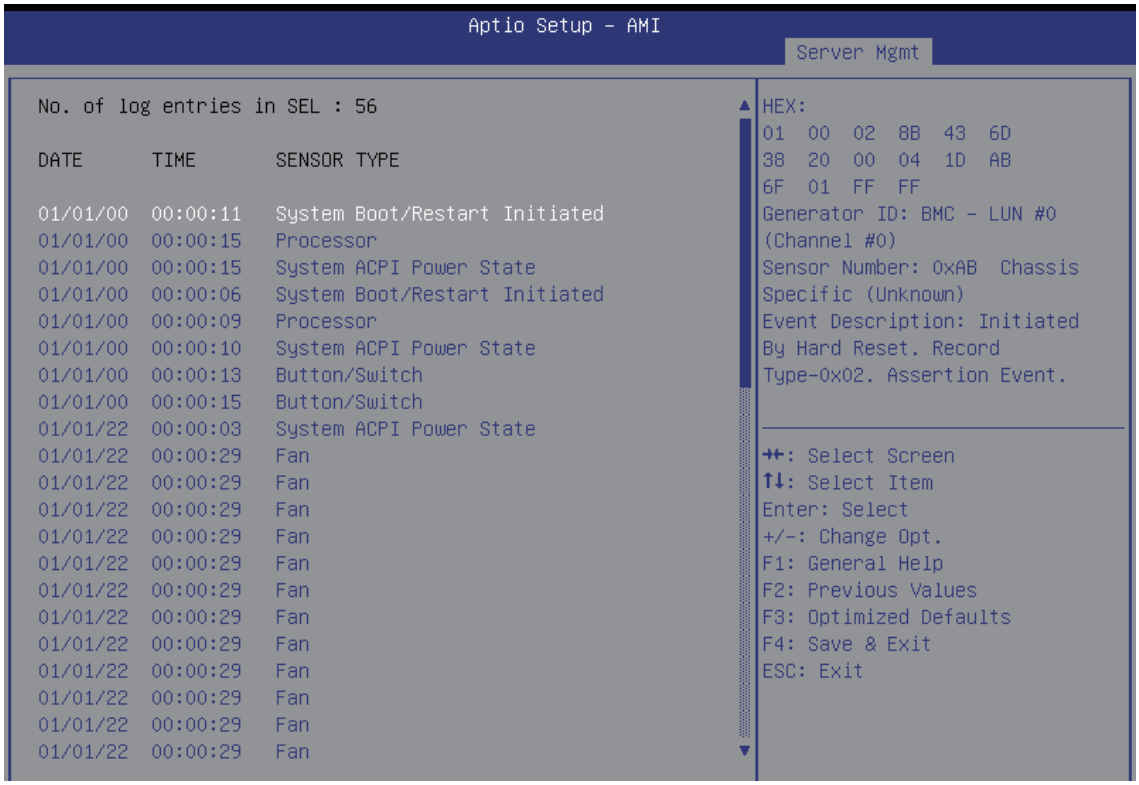


Figure 4-9-5 : View System Event Log

View the System Event Log Records.

4.9.6 BMC User Settings

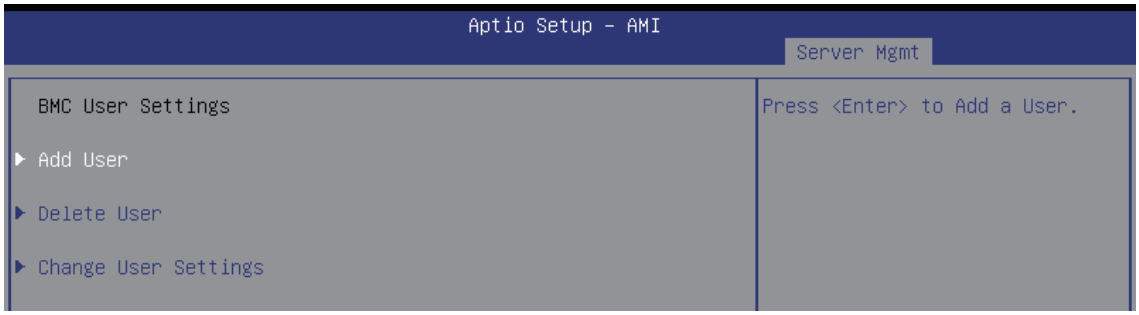


Figure 4-9-6 : BMC User Settings

Add, Delete and Set Privilege level for users.

5

SERVER MANAGEMENT

5.1 Audience

This chapter is intended for system administrators, integrators, and engineers responsible for configuring, managing, and maintaining the Baseboard Management Controller (BMC).

Readers are expected to have:

- A basic understanding of server hardware and system management concepts
- Familiarity with networking, IPMI, and Redfish interfaces
- Experience using command-line tools and web-based management interfaces

This guide assumes that users have appropriate access permissions to perform BMC-related configuration and management tasks.

5.2 Introduction

5.2.1 Overview

The Baseboard Management Controller (BMC) in VECOW servers provides remote management. It operates independently of the main system CPU, BIOS/ UEFI firmware and OS, allowing administrators to control and troubleshoot servers even when powered off.

The VECOW BMC complies with IPMI 2.0 and the Redfish v1.19.
Additionally, the BMC provides a web-based UI with secure HTTP (HTTPS) for server management including remote KVM and virtual media functions.

5.2.2 Management Interfaces

The BMC provides following interfaces for user to manage the server:

5.2.2.1 Out-of-Band Interfaces

Dedicated NIC
A separate network interface controller (NIC) exclusively for BMC management traffic.

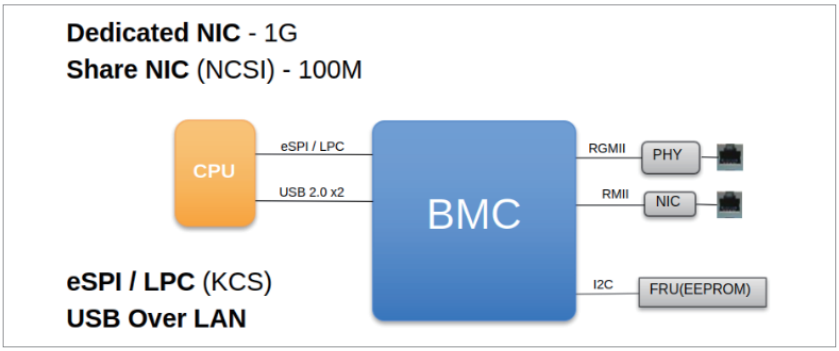
Shared NIC
The BMC utilizes the server's primary NIC for management traffic through the NCSI specification.

5.2.2.2 In-Band Interface

The BMC utilizes the server's primary NIC for management traffic through the NCSI specification.

eSPI
The Enhanced Serial Peripheral Interface (eSPI) with the Keyboard Controller Style (KCS) protocol allows the host system to communicate with the BMC.

USB Over LAN
The USB over LAN interface with the HTTPS/RMCP+ protocol allows the host system to communicate with the BMC over a network-like connection without requiring a physical network cable.



Note:
USB Over LAN requires appropriate driver support to function. It is currently compatible with Linux OS, and Windows Server 2019 and Windows Server 2022. (Please refer to the appendix for Windows driver installation.)
USB Over LAN hardware linkage is embedded within the server board, positioned between the CPU and the BMC SoC. Although it operates over a LAN interface, it is considered an in-band access method since the connection remains entirely within the server's internal architecture.

5.2.3 BMC Management Tools

This document utilizes major utilities such as IPMITool, Postman, and cURL to manage the server via the BMC.

Various tools are available to communicate with and manage the BMC, providing different levels of control and automation.

IPMITool
IPMITool is a command-line utility that allows users to interact with the BMC using the IPMI protocol. It enables remote management, power control, sensor monitoring, and event log retrieval.

Postman
Postman provides a user-friendly interface to send RESTful API requests to the BMC, leveraging the Redfish standard for server management.

Web Browser
The BMC offers a web-based user interface for server management. Users can easily navigate and perform management tasks using commonly used browsers such as Firefox, Chrome, and Edge.

5.2.4 Factory Default LAN Configuration

Dedicated NIC Interface

IPv4: Static IP configuration
Default IP Address: 192.168.10.11
Default Subnet Mask: 255.255.255.0
IPv6: DHCP by default

Shared NIC Interface

IPv4: DHCP by default
IPv6: DHCP by default

The Dedicated NIC and Shared NIC should not be configured on the same subnet. For example, avoid assigning the Shared NIC an IP like 192.168.10.x, which would overlap with the Dedicated NIC (192.168.10.11).

USB Over LAN Interface

IPv4: Static IP configuration
Default IP Address: 169.254.0.17
Default Subnet Mask: 255.255.0.0

5.3 IPMI Management

5.3.1 Overview

The VECOW BMC complies with the Intelligent Platform Management Interface (IPMI) 2.0 specification.

The IPMI specification defines a standardized approach for out-of-band server management, with the Baseboard Management Controller (BMC) as its core component. According to the specification, the BMC is designed to function independently of the server's main components, including the CPU, BIOS/UEFI firmware, and OS. This architectural design ensures that the BMC can continue to operate and respond to remote management commands even if the host system is powered off, unresponsive, or unbootable, as long as standby power is available.

This allows system administrators to perform critical tasks such as powering the system on or off, checking hardware health, and reviewing system logs remotely and reliably, without relying on the host software stack.

5.3.2 Getting Started

Use ipmitool to communicate with the BMC over the network or locally, allowing you to perform system monitoring, power control, and other remote management functions.

5.3.2.1 VECOW IPMI Default Credentials

Username: **vecow**
Password: **Vec0w@rz**

To issue IPMI commands locally, use the following format:

Syntax
ipmitool <Command>

To issue IPMI commands over the network using the LAN interface, use the following format:

Syntax

ipmitool -I lanplus -H <BMC_IP> -U <USERNAME> -P <PASSWORD> <COMMAND>

Parameters

- I lanplus: Specifies the interface (LAN with RMCP+ for IPMI 2.0)
- H <BMC_IP>: IPv4 or IPv6 address of the BMC
- U <USERNAME>: IPMI username
- P <PASSWORD>: IPMI password
<COMMAND>: The operation to perform (e.g., power status, sensor list, etc.)

```
Commands:
        raw             Send a RAW IPMI request and print response
        i2c             Send an I2C Master Write-Read command and print response
        spd             Print SPD info from remote I2C device
        lan             Configure LAN Channels
        chassis         Get chassis status and set power state
        power           Shortcut to chassis power commands
        event           Send pre-defined events to MC
        mc              Management Controller status and global enables
        sdr             Print Sensor Data Repository entries and readings
        sensor          Print detailed sensor information
        fru             Print built-in FRU and scan SDR for FRU locators
        gendev          Read/Write Device associated with Generic Device locators sdr
        sel             Print System Event Log (SEL)
        pef             Configure Platform Event Filtering (PEF)
        sol             Configure and connect IPMIv2.0 Serial-over-LAN
        tsol            Configure and connect with Tyan IPMIv1.5 Serial-over-LAN
        isol            Configure IPMIv1.5 Serial-over-LAN
        user            Configure Management Controller users
        channel         Configure Management Controller channels
        session         Print session information
        dcmi            Data Center Management Interface
        nm              Node Manager Interface
        sunoem          OEM Commands for Sun servers
        kontronoem      OEM Commands for Kontron devices
        picmg           Run a PICMG/ATCA extended cmd
        fwum            Update IPMC using Kontron OEM Firmware Update Manager
        firewall        Configure Firmware Firewall
        delloem         OEM Commands for Dell systems
        shell           Launch interactive IPMI shell
        exec            Run list of commands from file
        set             Set runtime variable for shell and exec
        hpm             Update HPM components using PICMG HPM.1 file
        ekanalyzer      run FRU-Ekeying analyzer using FRU files
        ime             Update Intel Manageability Engine Firmware
        vita            Run a VITA 46.11 extended cmd
        lan6            Configure IPv6 LAN Channels
```

5.3.3 Chassis Power Control

Use ipmitool to execute the IPMI Chassis Control Command to take power action of the server.

Syntax

ipmitool chassis power <action>

Parameters

<action>: The power operation to perform. Supported actions include:
status – Show current power status
on – Power on the chassis
off – Power off the chassis (forced power off the system)
cycle – Power cycle the chassis (off, then on)
soft – graceful shutdown the system (equivalent to pressing the power button)
reset – Reset the system (equivalent to pressing the reset button)

The following illustrates the power control command.

ipmitool -I lanplus -H 192.168.10.11 -U vecow -P Vec0w@rz chassis power on
ipmitool -I lanplus -H 192.168.10.11 -U vecow -P Vec0w@rz chassis power off
ipmitool -I lanplus -H 192.168.10.11 -U vecow -P Vec0w@rz chassis power cycle

5.3.4 Sensor Monitoring

Use ipmitool to execute the IPMI Sensor Device Commands to retrieve system health data, such as temperature, voltage, fan speed, and other critical hardware health parameters from the server.

Syntax

ipmitool sdr elist

Parameter

sdr elist: The Sensor Data Records (SDR) list command to fetch sensor health data

The following figure illustrates the result of the command.

```
$ ipmitool -I lanplus -H 192.168.10.24 -U vecow -P Vec0w@rz sdr elist
CPU_Temp         | 06h | ok  |  3.1 | 32 degrees C
DIMM_Temp        | 08h | ok  | 32.1 | 29 degrees C
CPU_VR0_Temp     | 0Ah | ok  |  7.1 | 33 degrees C
CPU_VR1_Temp     | 0Bh | ok  |  7.2 | 39 degrees C
CPU_VR2_Temp     | 0Ch | ok  |  7.3 | 32 degrees C
SYS_12V          | 30h | ok  |  7.4 | 12.09 Volts
SYS_5V           | 31h | ok  |  7.5 | 5.12 Volts
SYS_3.3V         | 32h | ok  |  7.6 | 3.35 Volts
P3V_BAT          | 33h | ok  | 40.1 | 3.03 Volts
CPU_VCORE0       | 37h | ok  |  3.2 | 1.10 Volts
CPU_VCORE1       | 38h | ok  |  3.3 | 1.04 Volts
CPU_Power        | 40h | ok  |  3.4 | 4 Watts
MEM_Power        | 41h | ok  | 32.2 | 1 Watts
P12_STBY_Power   | 4Ah | ok  |  7.7 | 25 Watts
P12_BP1_Power    | 4Bh | ns  | 16.1 | Disabled
P12_BP2_Power    | 4Ch | ns  | 16.2 | Disabled
FAN0_CPU         | 20h | ok  | 29.1 | 2520 RPM
FAN1_MB          | 22h | ok  | 29.2 | 6120 RPM
FAN2_MB          | 24h | ok  | 29.3 | 6120 RPM
FAN3_MB          | 26h | ok  | 29.4 | 6180 RPM
FAN4_MB          | 28h | ok  | 29.5 | 6120 RPM
FAN5_IO          | 2Ah | ok  | 29.6 | 3090 RPM
FAN6_IO          | 2Ch | ok  | 29.7 | 3120 RPM
CPU_Status       | 35h | ok  |  3.5 | Presence detected
ACPI_State       | A8h | ok  |  5.7 | S0/G0: working
Event_Log        | E1h | ok  |  6.2 |
Watchdog2        | AFh | ok  |  6.3 |
```

Note:
Please contact VECOW for detailed IPMI project-specific platform sensor specification.

5.3.5 Serial Over LAN (SOL)

SOL is a feature that allows remote redirection of the server's serial port over a network connection.

This feature is particularly useful for administrators to access the system's console remotely without needing to be physically present at the server or having a direct serial cable connection.

To activate the SOL console, use the following command:

Syntax

ipmitool -I lanplus -H <BMC_IP> -U <USERNAME> -P <PASSWORD> sol activate

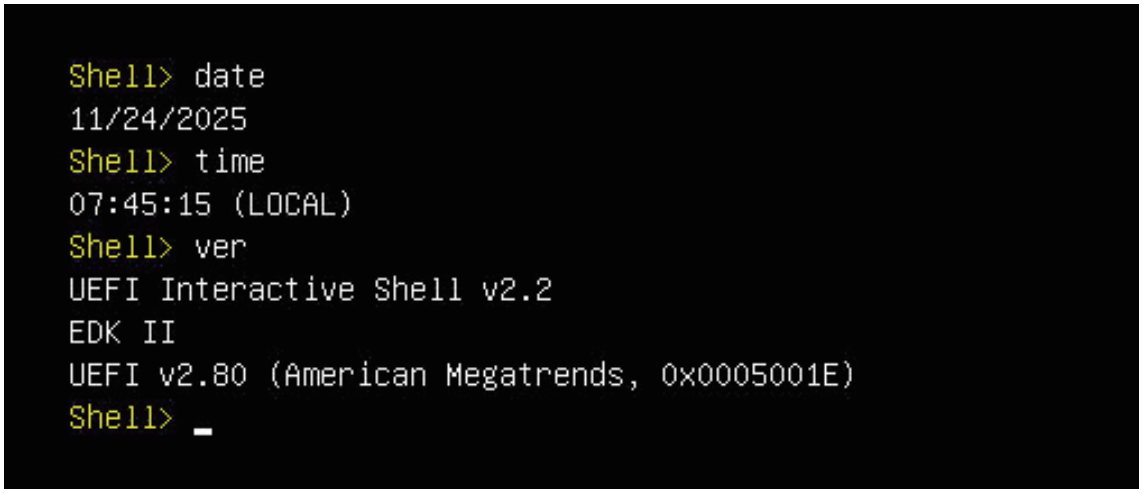
Parameter

sol activate: Activates the SOL session, redirecting the serial port over the network.

The following figure illustrates the SOL activation command.

```
$ ipmitdate-I lanplus -H 192.168.10.24 -U vecow -P Vec0w@rz sol activate
11/24/2025on operational.  Use ~? for help]
Shell> time
07:45:15 (LOCAL)
Shell> ver
UEFI Interactive Shell v2.2
EDK II
UEFI v2.80 (American Megatrends, 0x0005001E)
Shell>
```

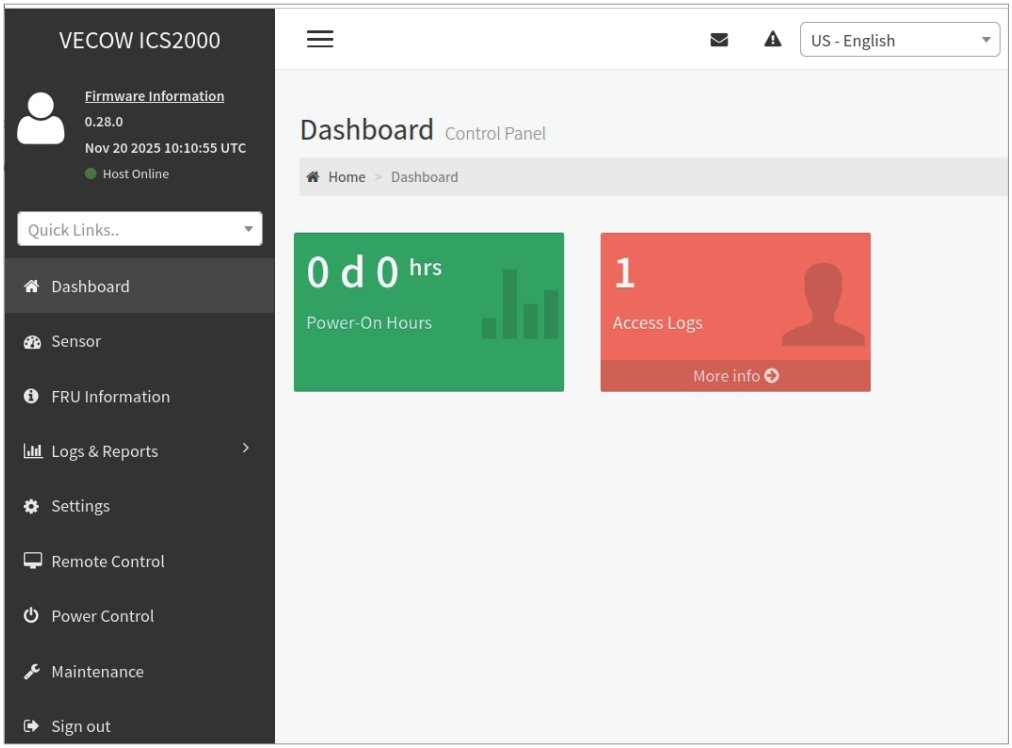
The image below shows the physical monitor display, which is synchronized with the SOL (Serial over LAN) console.



5.4 WebUI Management

The BMC offers a web-based user interface that simplifies server management.

Administrators can remotely monitor system health, configure settings, update firmware, control power states, and review event logs, all secured via an HTTPS connection to ensure privacy and data integrity.



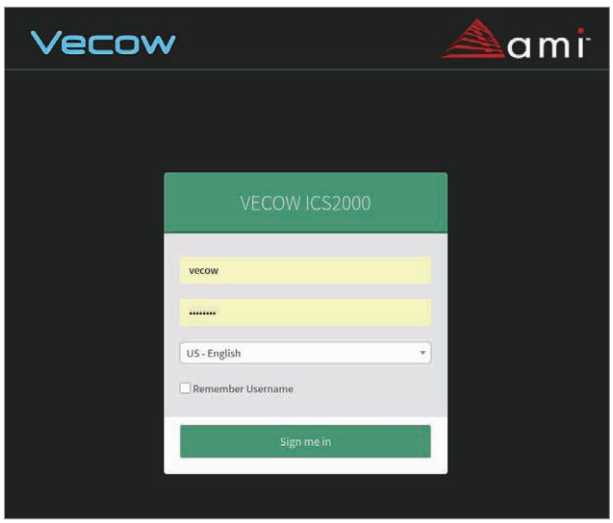
5.4.1 Getting Started

Use BMC's IPv4 or IPv6 IP address with HTTPS protocol to access the BMC WebUI. Enter the default VECOW IPMI default credentials to login to the WebUI.

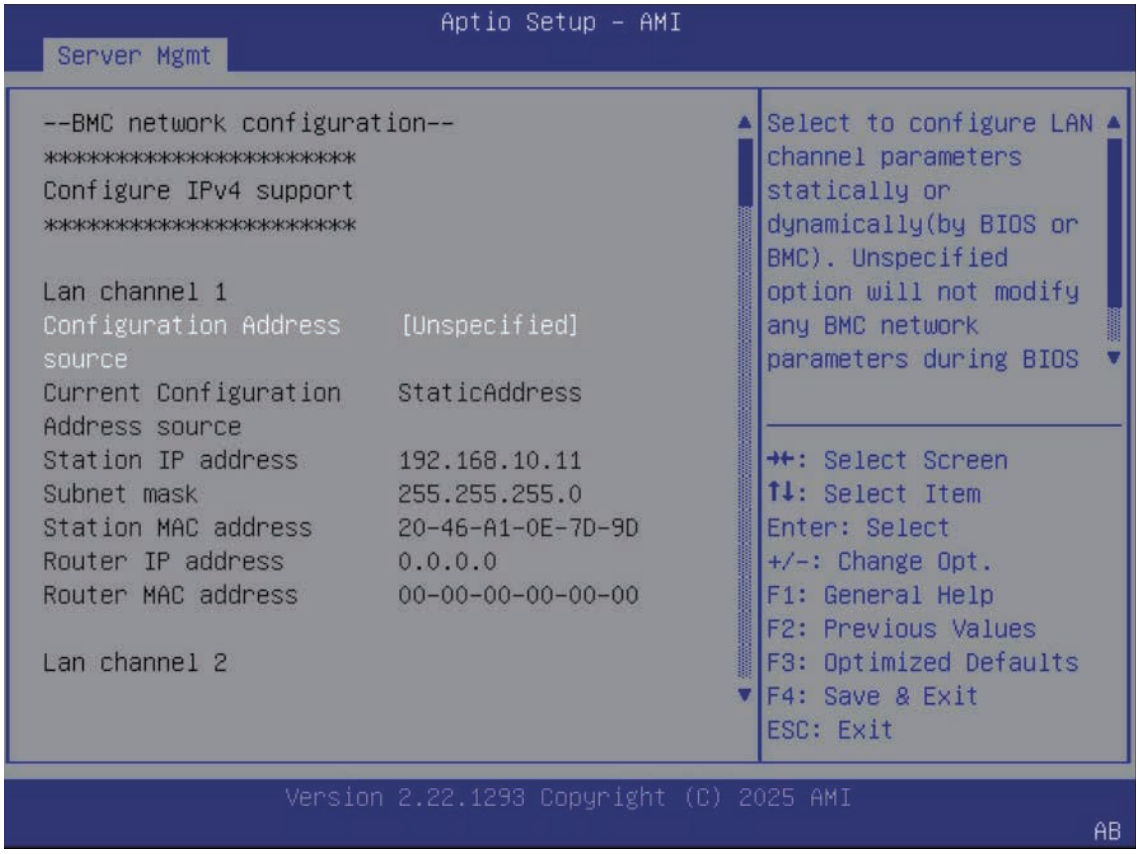
5.4.1.1 VECOW IPMI Default Credentials

Username: **vecow**
Password: **Vec0w@rz**

The BMC WebUI and IPMI credentials are shared, meaning the same credentials are used for both the web interface and IPMI access.

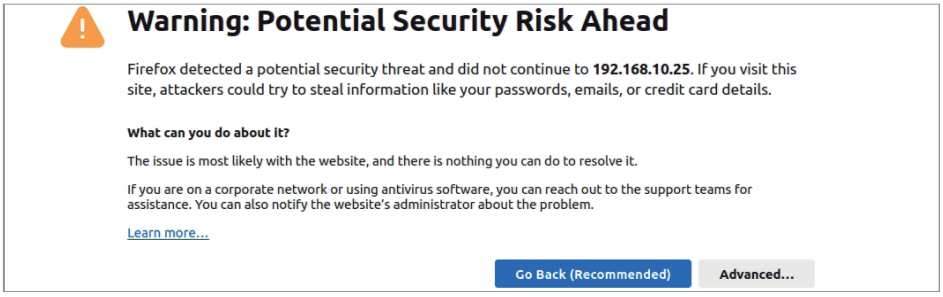


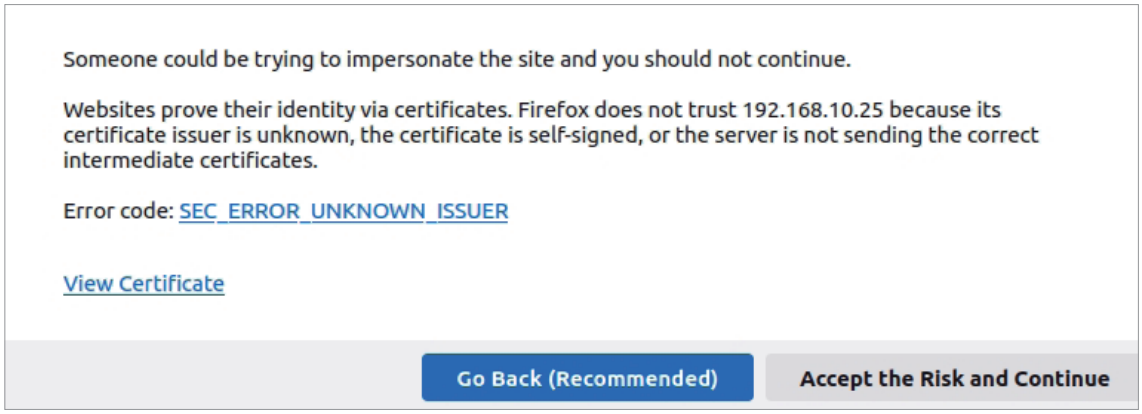
The following figure illustrates how to retrieve the BMC IP address from the BIOS menu.



Note:

The first time you login to the BMC WebUI, a security warning may appear. To proceed, click “Advanced”, then choose to accept to navigate the login page.

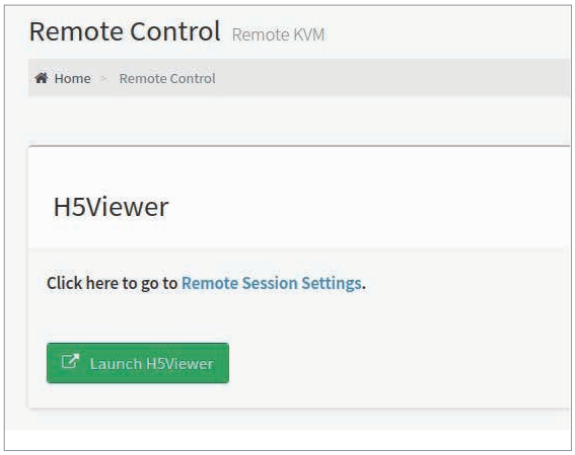




5.4.2 Remote KVM

The remote KVM feature is OS-independent and mirrors the exact display shown on the physical monitor connected to the system, including BIOS boot screens, BIOS setup menus, and the OS's GUI.

Power on the system, then navigate to the **Remote Control** page.
Clicking the "Launch H5Viewer" button to start the remote KVM console.



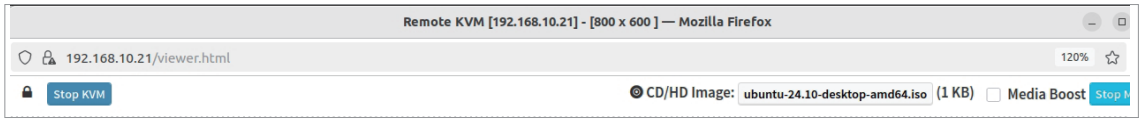

```
Mapping table
     BLK0: Alias(s):
          PciRoot(0x0)/Pci(0x7,0x1)/Pci(0x0,0x4)/USB(0x0,0x0)/USB(0x1,0x0)
     BLK4: Alias(s):
          PciRoot(0x0)/Pci(0x7,0x1)/Pci(0x0,0x4)/USB(0x0,0x0)/USB(0x2,0x0)
     BLK1: Alias(s):
          PciRoot(0x0)/Pci(0x7,0x1)/Pci(0x0,0x4)/USB(0x0,0x0)/USB(0x1,0x0)/Unit(
0x1)
     BLK2: Alias(s):
          PciRoot(0x0)/Pci(0x7,0x1)/Pci(0x0,0x4)/USB(0x0,0x0)/USB(0x1,0x0)/Unit(
0x2)
     BLK3: Alias(s):
          PciRoot(0x0)/Pci(0x7,0x1)/Pci(0x0,0x4)/USB(0x0,0x0)/USB(0x1,0x0)/Unit(
0x3)
     BLK5: Alias(s):
          PciRoot(0x0)/Pci(0x7,0x1)/Pci(0x0,0x4)/USB(0x0,0x0)/USB(0x2,0x0)/Unit(
0x1)
     BLK6: Alias(s):
          PciRoot(0x0)/Pci(0x7,0x1)/Pci(0x0,0x4)/USB(0x0,0x0)/USB(0x2,0x0)/Unit(
0x2)
     BLK7: Alias(s):
          PciRoot(0x0)/Pci(0x7,0x1)/Pci(0x0,0x4)/USB(0x0,0x0)/USB(0x2,0x0)/Unit(
0x3)
Press ESC in 1 seconds to skip startup.nsh or any other key to continue.
Shell> _
```

5.4.3 Remote Media

The remote media feature is OS-independent. The BMC firmware simulates storage media through a USB hub connected to the CPU, functioning as if a USB storage device were physically plugged in by the user.

Select an OS ISO file from your local computer through the remote console, then click the “Start Media” button to begin mounting.

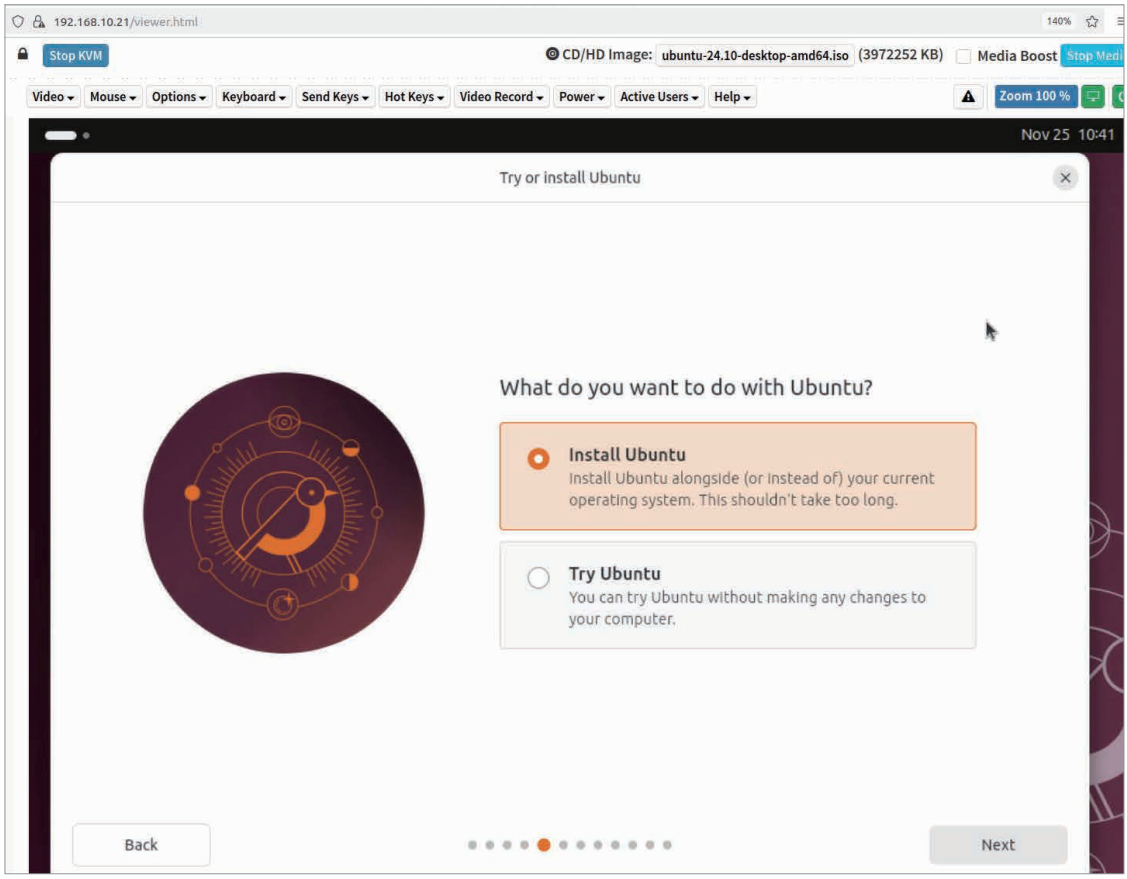
The following demonstration shows how to remotely mount a Linux installation ISO, then restart the server to initiate the Linux installation process.



Reboot the system into the BIOS setup menu to select the AMI virtual media to boot.



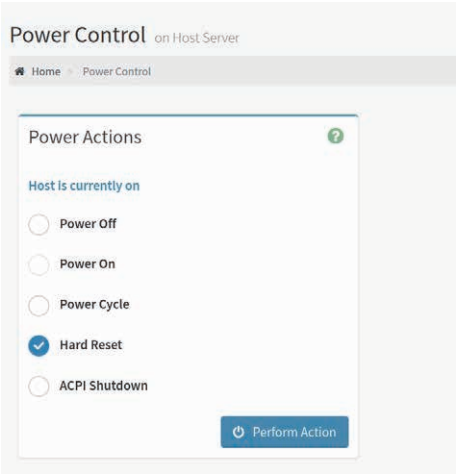
The system will then boot from the AMI virtual media mounted with the ISO file.



5.4.4 Chassis Power Control

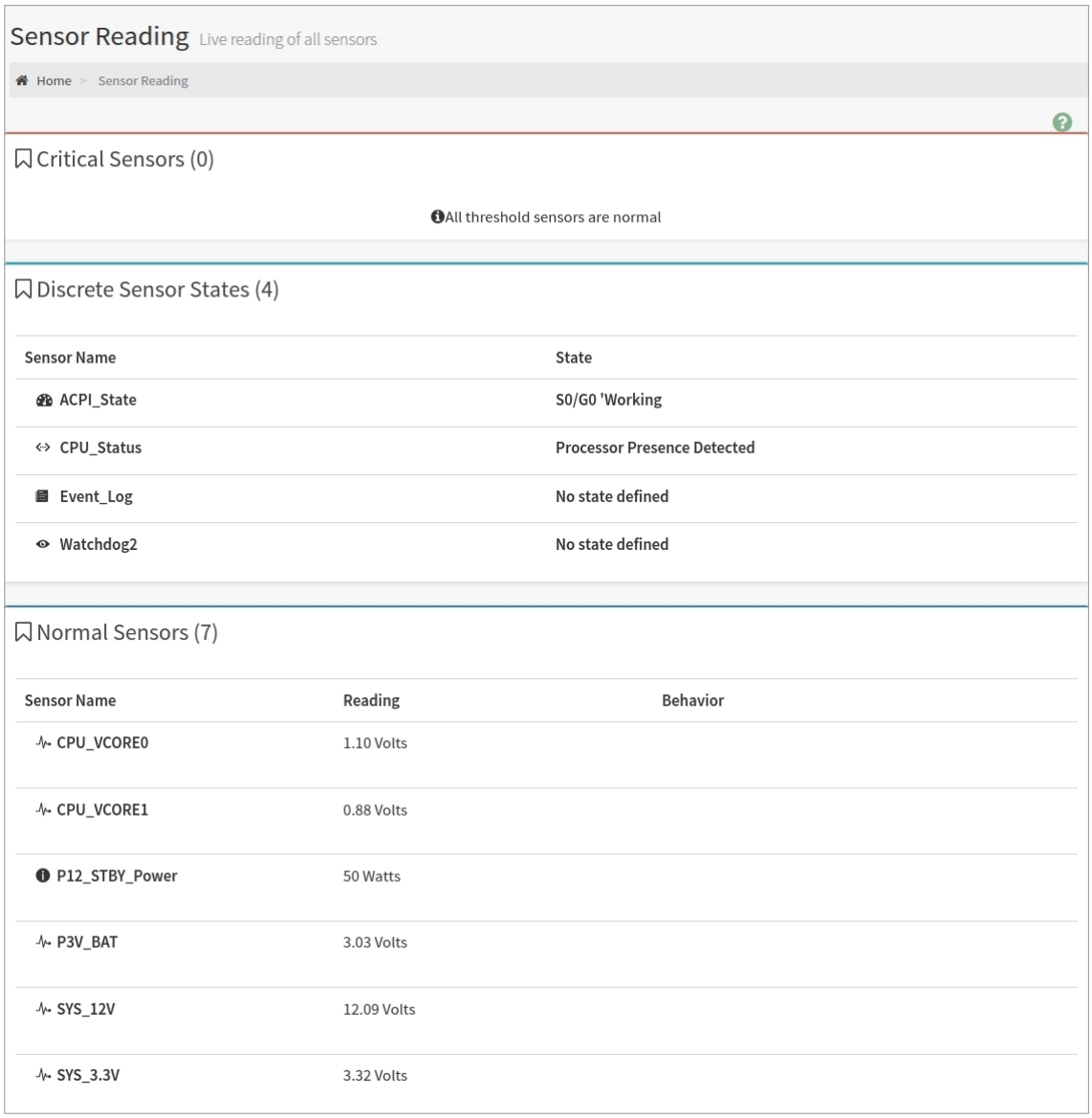
Navigate to the **Power Control** page.

Review the current power status of the server, then select the desired power control options by checking the corresponding checkboxes.



5.4.5 Sensor Monitoring

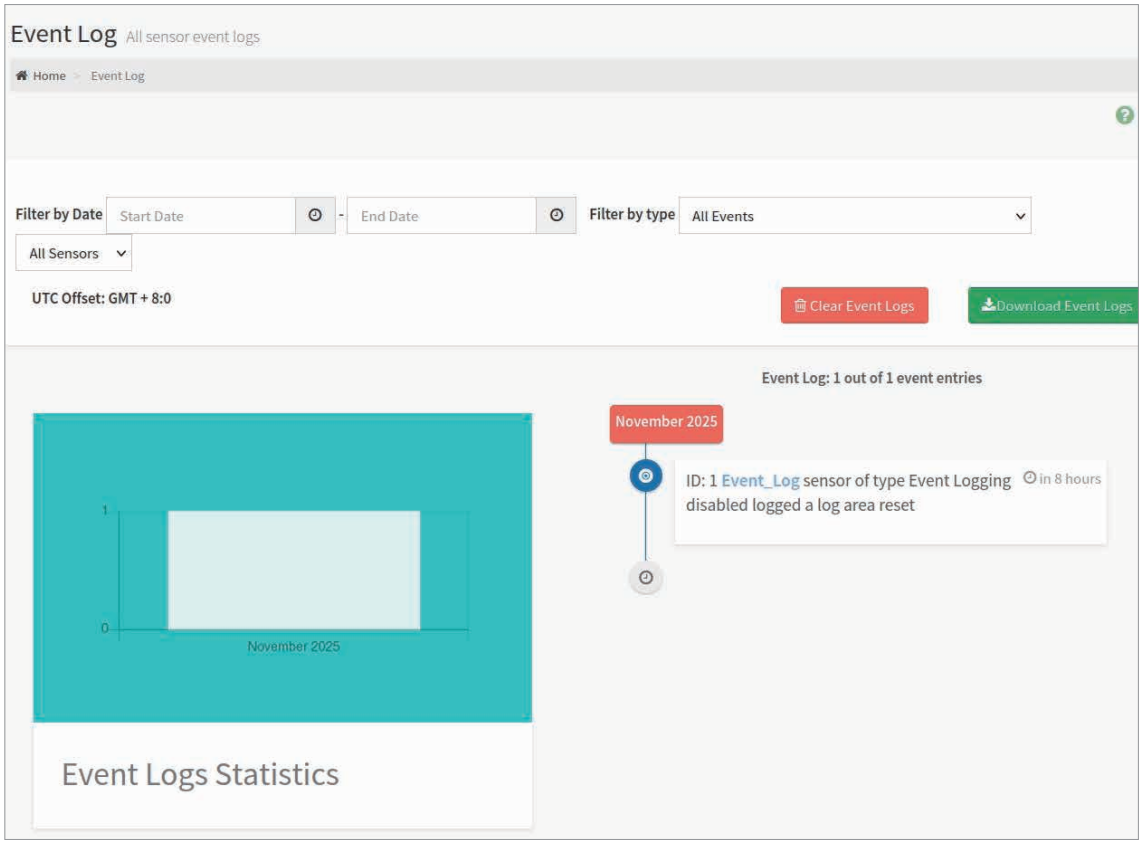
Navigate to the **Sensor** page.



5.4.6 Sensor Event Log (SEL)

Navigate to the **Logs and Reports > IPMI Event Log** page.

This page displays IPMI SEL entries triggered when a predefined sensor threshold is crossed or when specific sensor events occur.



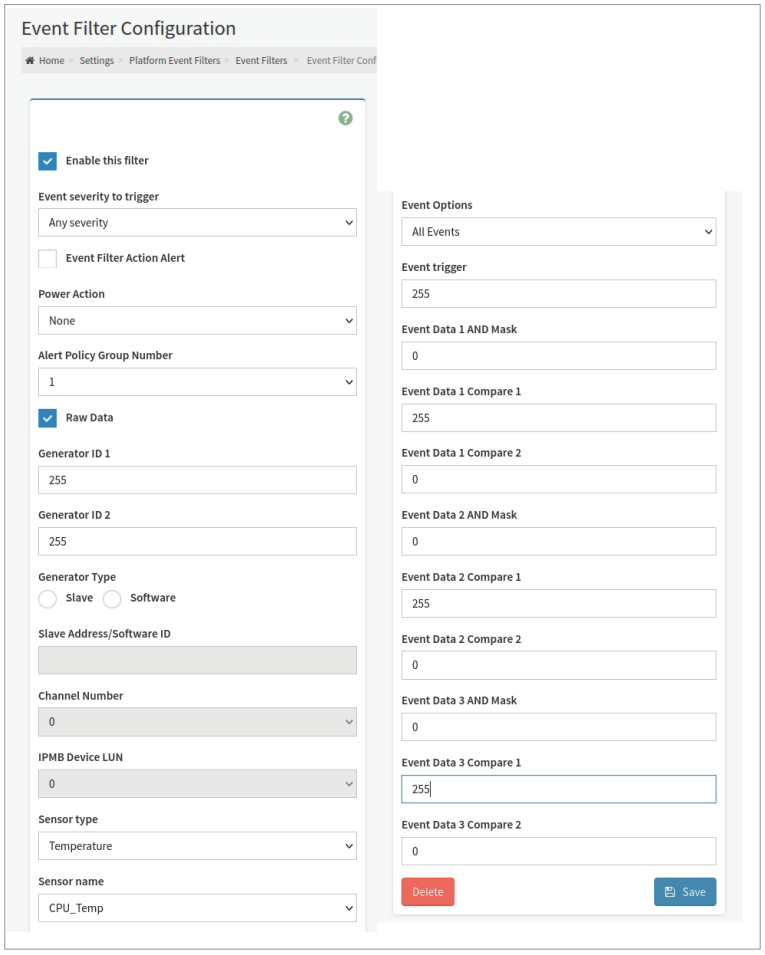
Note:
The SEL timestamps may be incorrect if the BMC time is not synchronized with the BIOS or an NTP server.
Once the BMC firmware time is synchronized, newly generated SEL entries will have correct timestamps.

5.4.7 Platform Event Filter (PEF)

When Sensor Event Log entry is generated and it matches the PEF configuration, an alert such as SNMP trap, or OEM Email will be sent to the specified destination.

Navigate to the **Settings > Platform Event Filter > Event Filters** page.

The following figure illustrates the "CPU_Temp" sensor as an example. When a threshold-crossing event occurs, an alert will be sent.

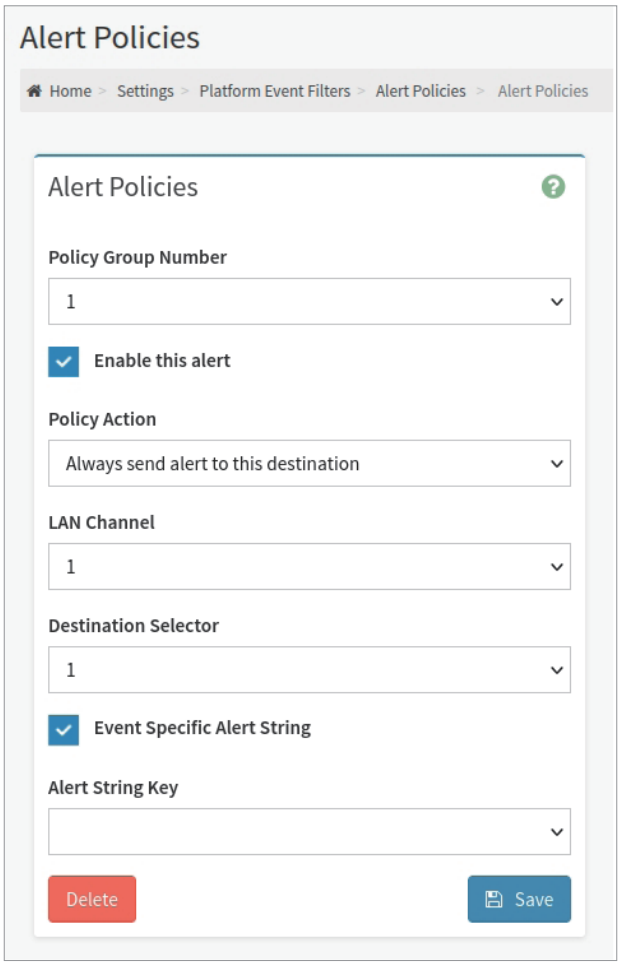


Alternatively, other PEF actions can be selected to proceed, including:
None
Power Down
Power Cycle
Power Reset
OEM Action

If the OEM action is selected to proceed, the following alert policy and destination need to be properly configured for either SNMP trap or OEM Email alert.

Navigate to the **Settings > Platform Event Filter > Alert Polices** page.

This page configuration links the **Policy Group Number** to a **Destination Selector**, which specifies either the IPMI user's email ID to receive the alert email, or the IP address of SNMP receiver to capture the trap message.



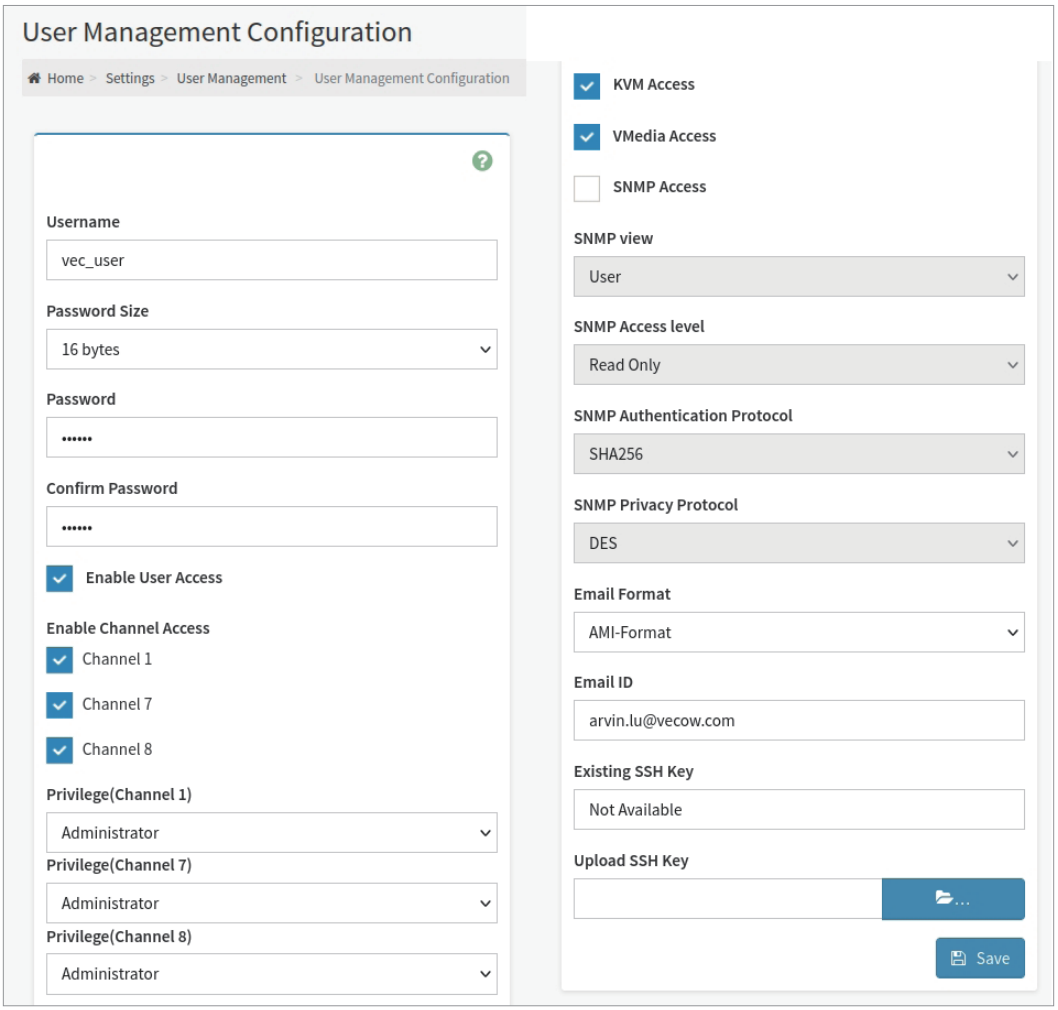
Above steps configure the event source for the PEF action.

The following section describes how to configure the PEF action of SNMP Alert, and OEM Mail Alert.

Email Alert

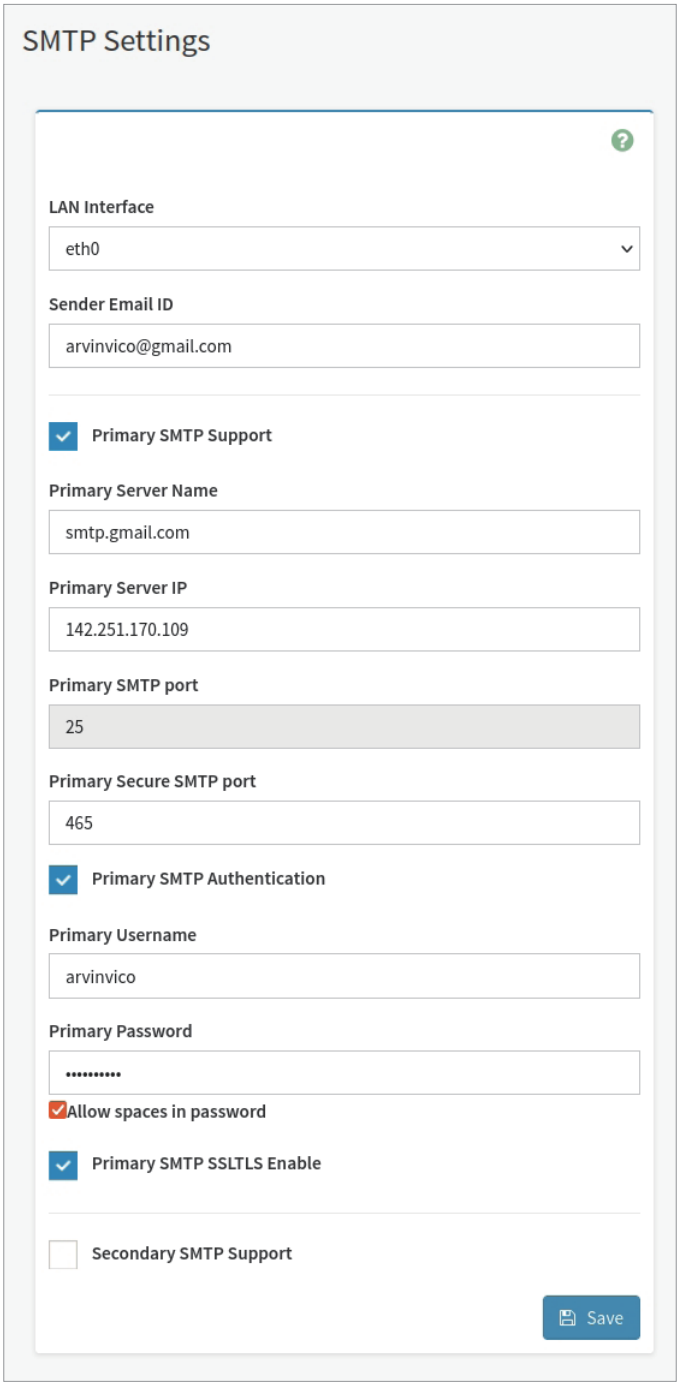
Navigate to **Settings > User Management** page.

Add an IPMI user with an email ID to which alert notifications will be sent.



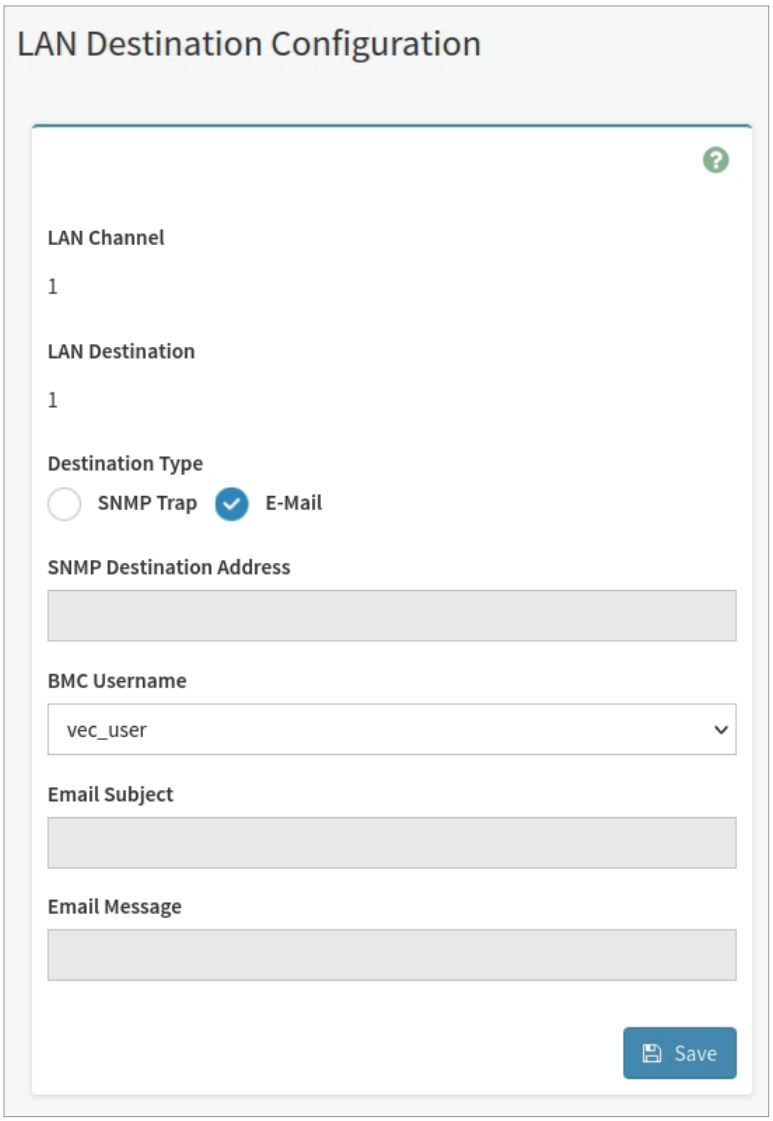
Navigate to the **Settings > SMTP Settings** page.

Specify an SMTP server to enable alert email delivery. The following figure shows an example using Gmail's SMTP server.



Navigate to the **Settings > Platform Event Filter > LAN Destination Configuration** page.

Configure the **LAN destination** to use the email address of the previously created IPMI user, **vec_user**, for example.





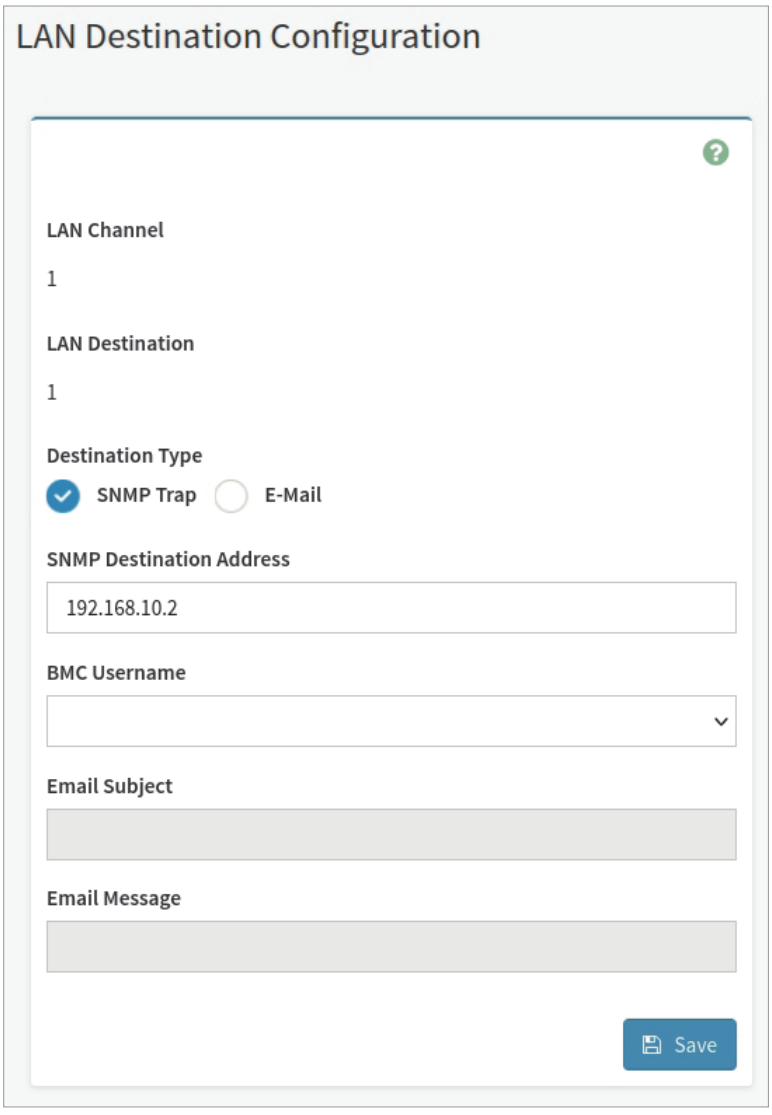
The following figure illustrates that when **CPU_Temp** sensor upper non-critical event occurs, an alert email will be sent to the email address of the IPMI user, **vec_user**.

SNMP Alert

Navigate to the **Settings > Platform Event Filter > LAN Destination Configuration** page.

Configure the **LAN destination** to use the IP address of the SNMP receiver.

The following figure illustrates that when **CPU_Temp** sensor upper non-critical event occurs, an alert SNMP trap will be sent to the IP address, *192.168.10.2*, where the snmptrapd service on the Linux OS will receive it.

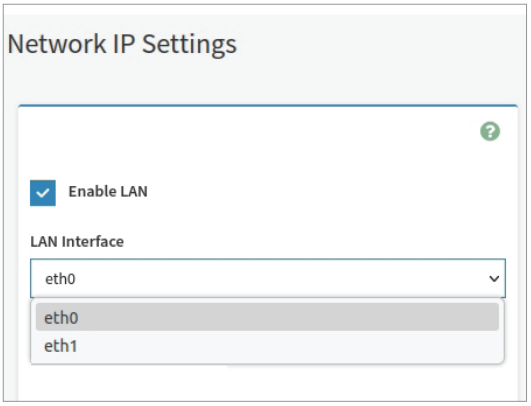


5.4.8 Network Channel Configuration

Navigate to the **Settings > User Management** page.

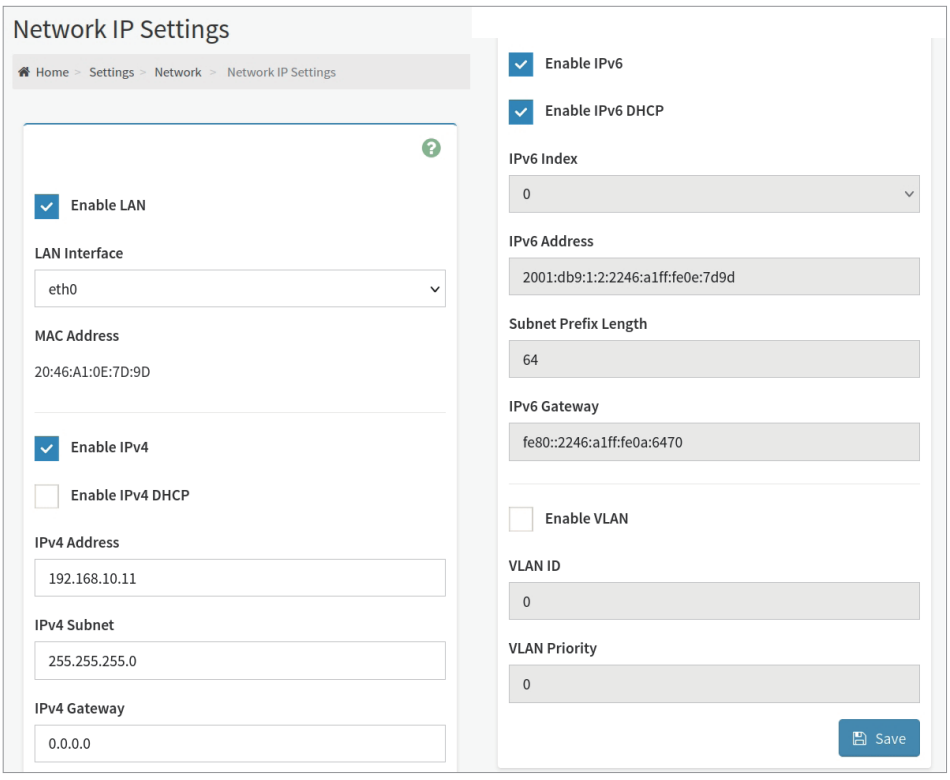
The BMC supports two LAN interfaces:
Channel 1 corresponds to eth0 (Dedicated NIC),
Channel 8 to eth1 (Shared NIC).

Users can select either LAN interface to view or modify its settings.



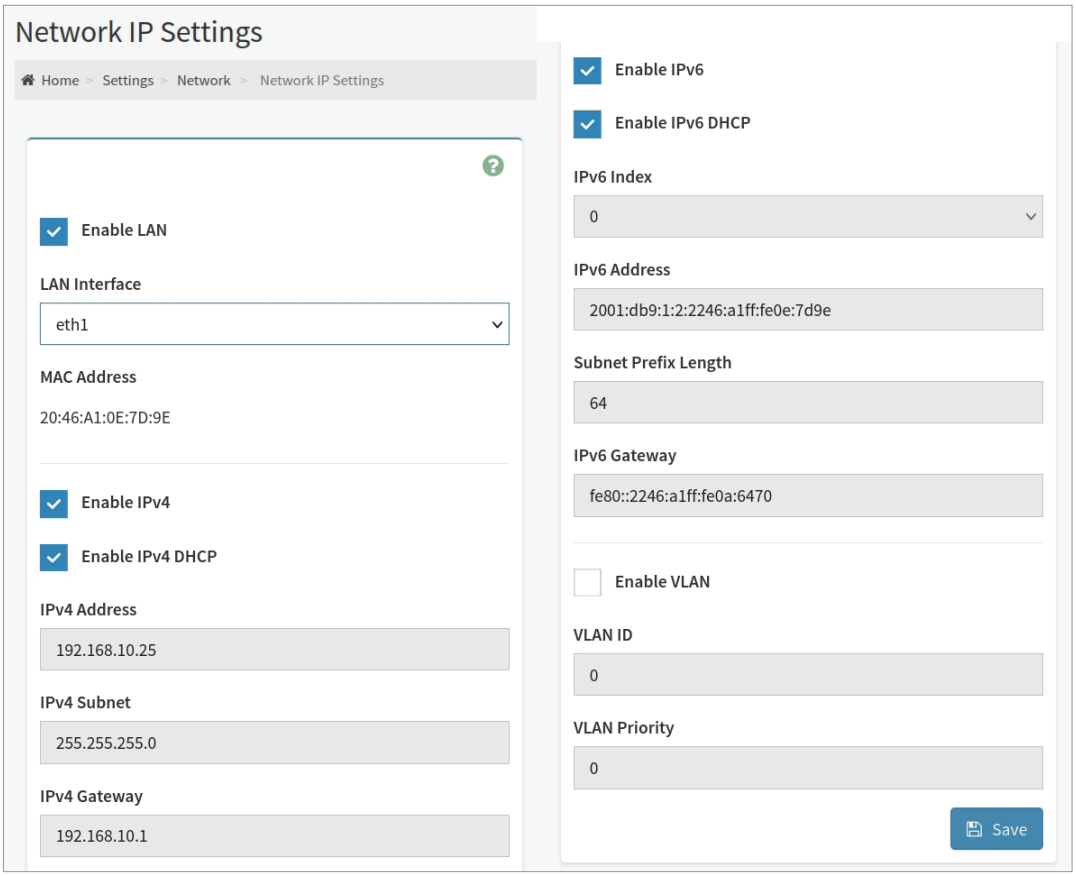
The following figure illustrates the default settings for the dedicated NIC.

IPv4: Static IP configuration
Default IP Address: 192.168.10.11
Default Subnet Mask: 255.255.255.0
IPv6: DHCP by default



The following figure illustrates the default settings for the shared NIC.

IPv4: DHCP by default
IPv6: DHCP by default



5.4.9 DNS Configuration

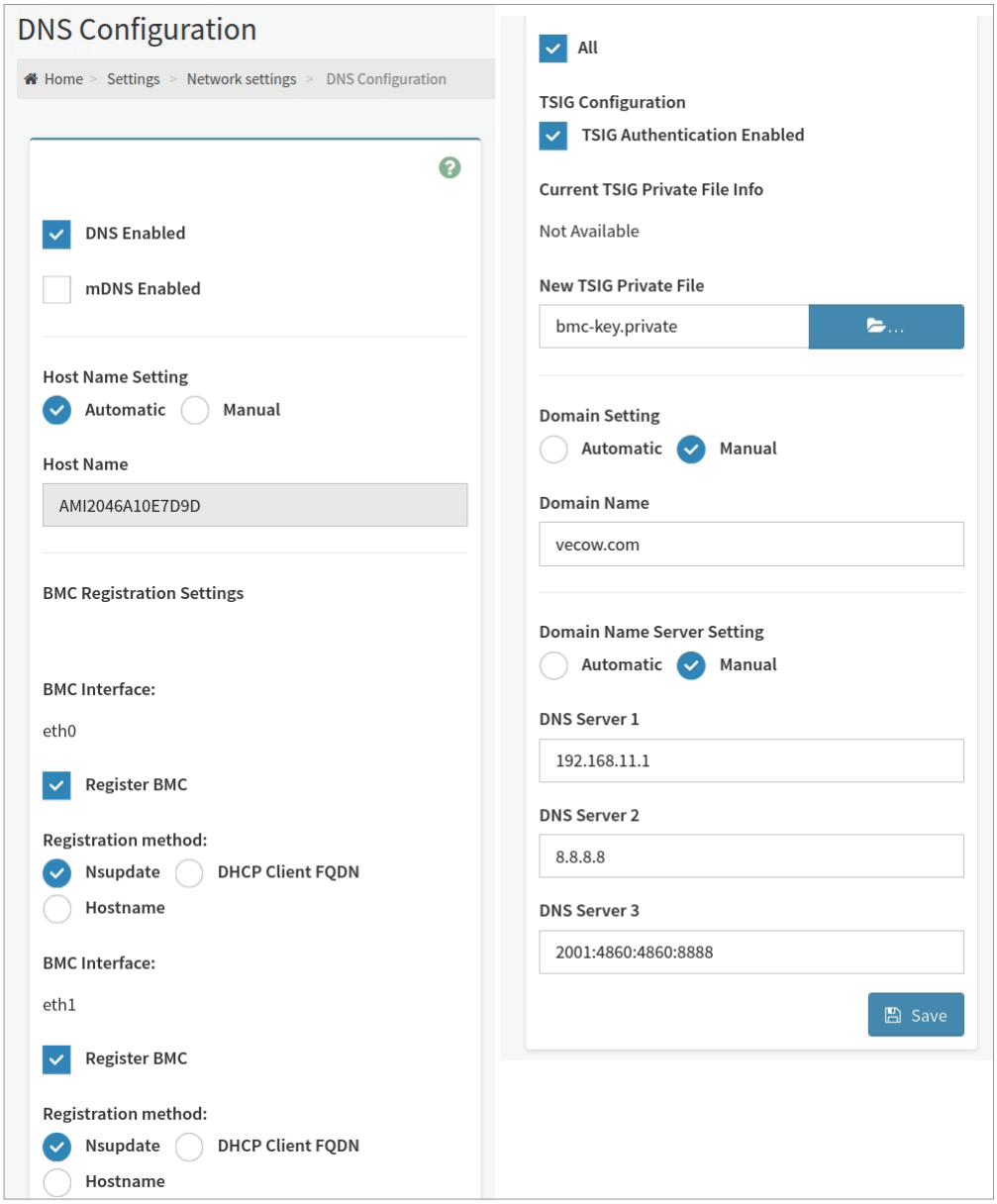
Navigate to the **Settings > Network Settings > DNS Configuration** page.

This page is used to configure the BMC's DNS.settings.

Select DNS Enabled checkbox.

The BMC DNS functionality supports device names, DNS registration methods (such as nsupdate, DHCP client FQDN, or Hostname), TSIG authentication, and domain name server configuration.

Note:
It is recommended to use BIND as the DNS server.



5.4.10 User Configuration

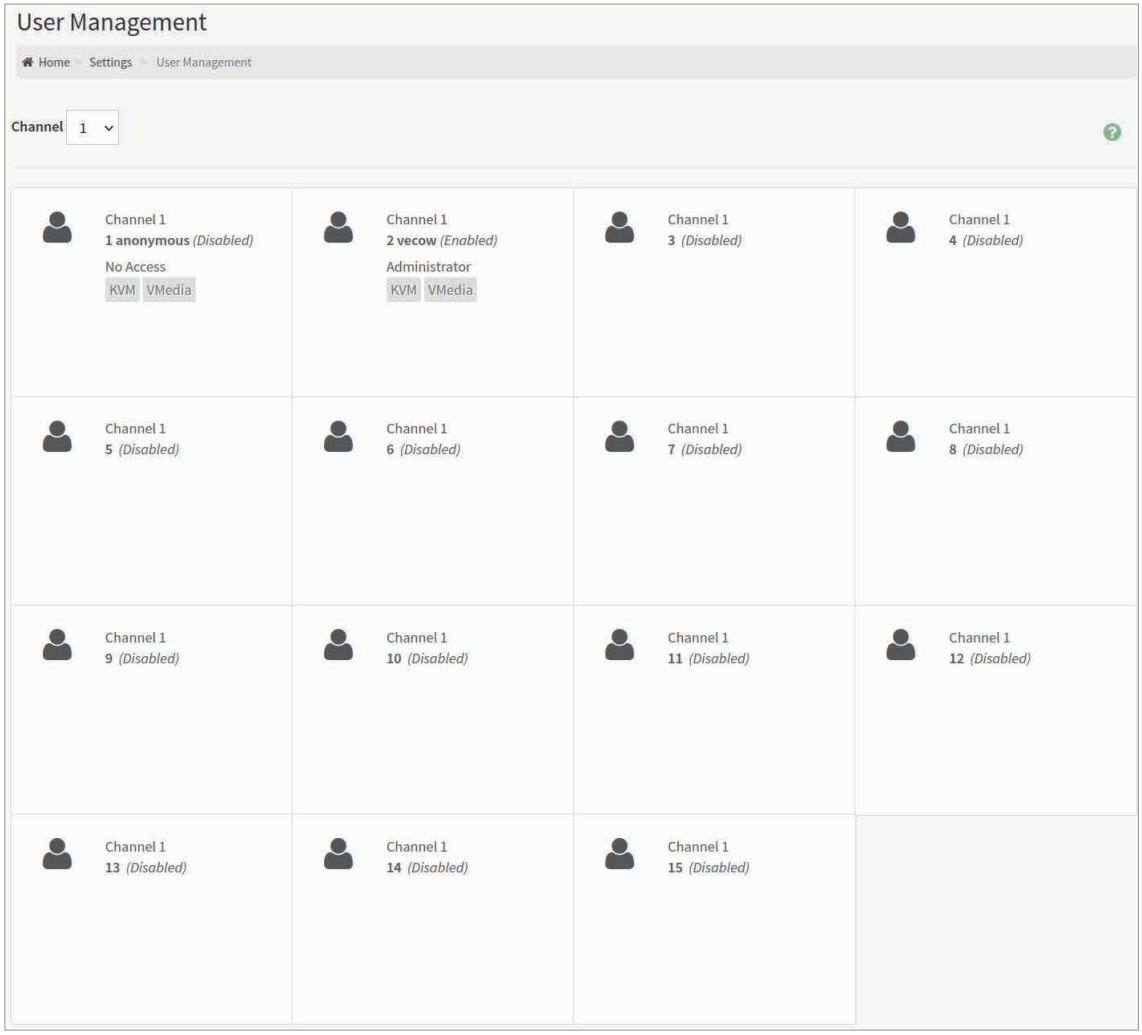
5.4.10.1 IPMI User Configuration

Navigate to the **Settings > User Management** page.

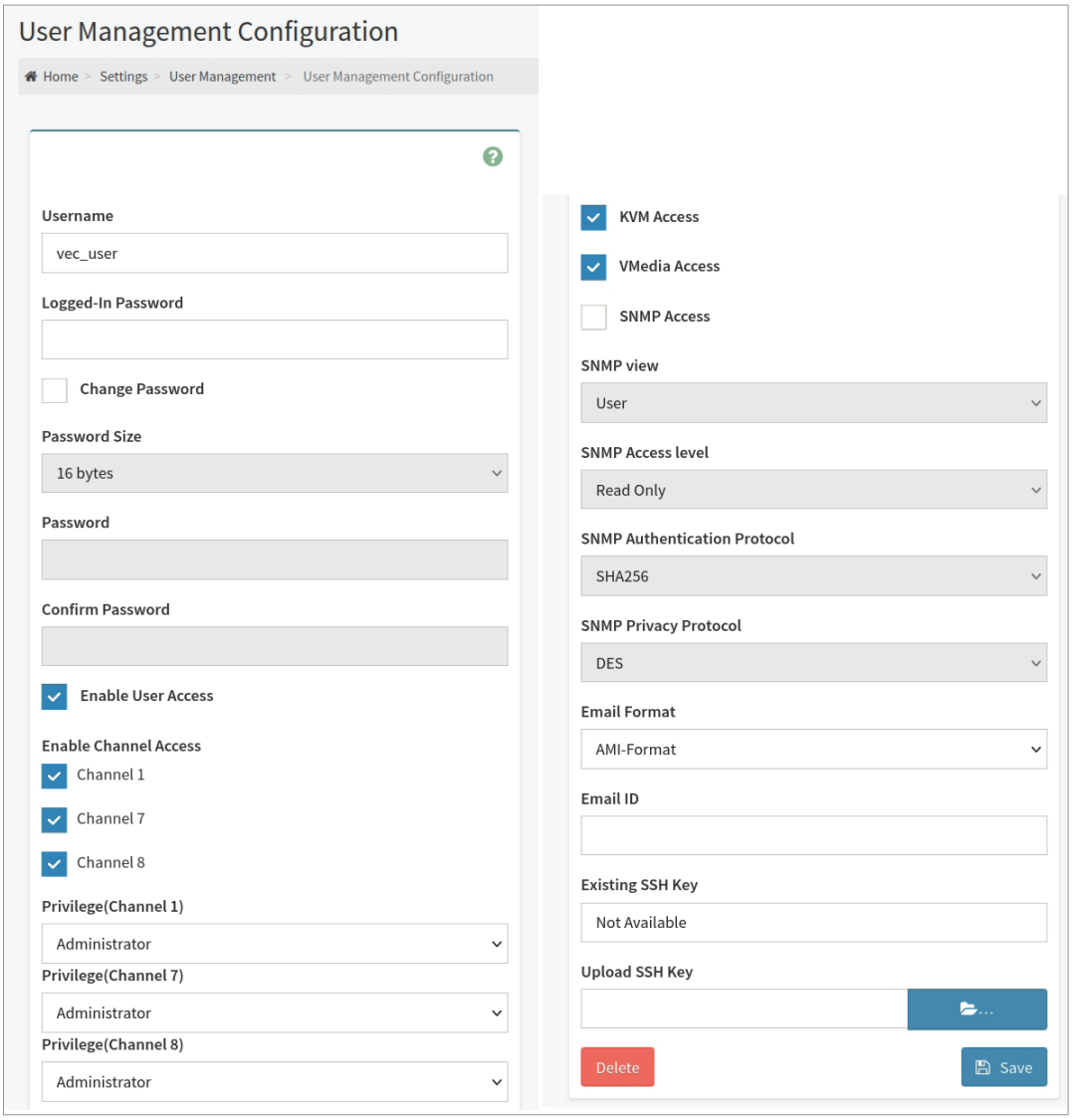
This page allows you to manage IPMI user accounts, including viewing, adding, editing, and removing users.

The 1st IPMI user account is preserved.
The 2nd IPMI user account is predefined as an Administrator.

IPMI user accounts are channel-specific; select a channel to view the corresponding user accounts.



The following figure demonstrates how to enable an IPMI user account.

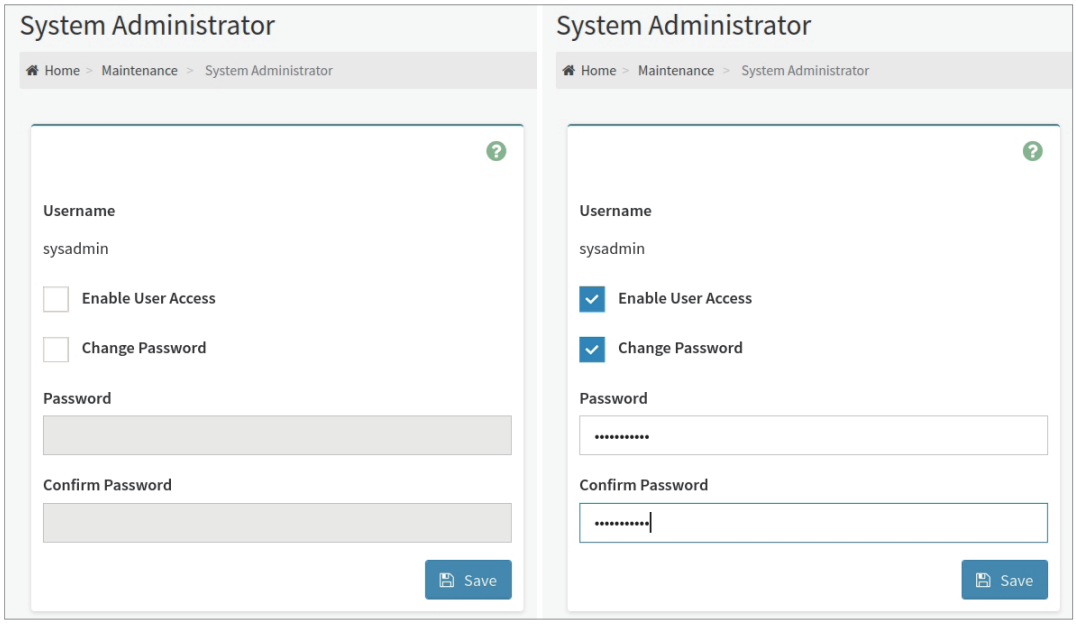


5.4.10.2 Superuser Configuration

Navigate to the **Maintenance > System Administrator** page.

The system administrator account is a BMC superuser and operates independently from the IPMI user accounts.
The superuser account is intended for advanced operations and firmware debugging purposes.

It is strongly recommended that users either disable the superuser account or change the default superuser password for security reasons.

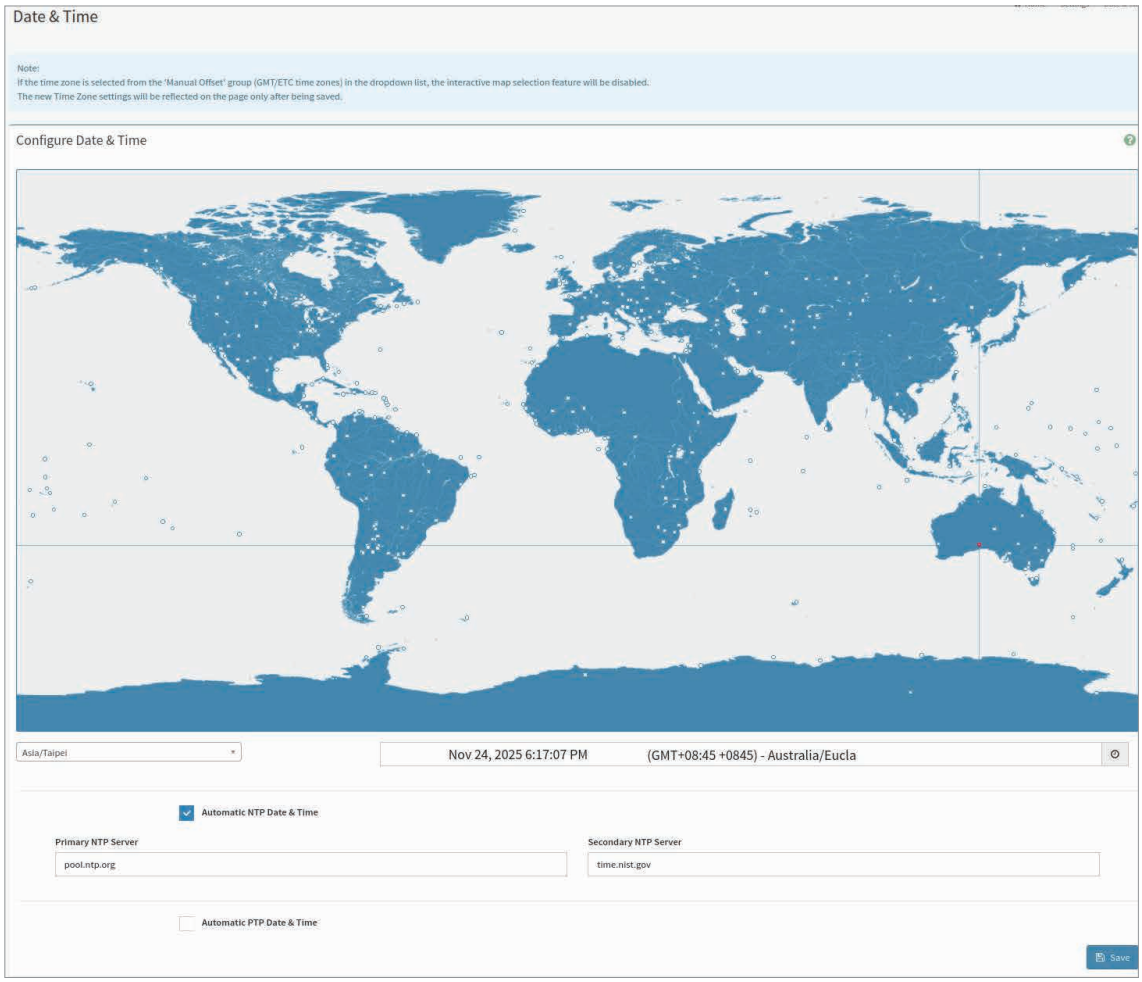


5.4.11 Date and Time Configuration

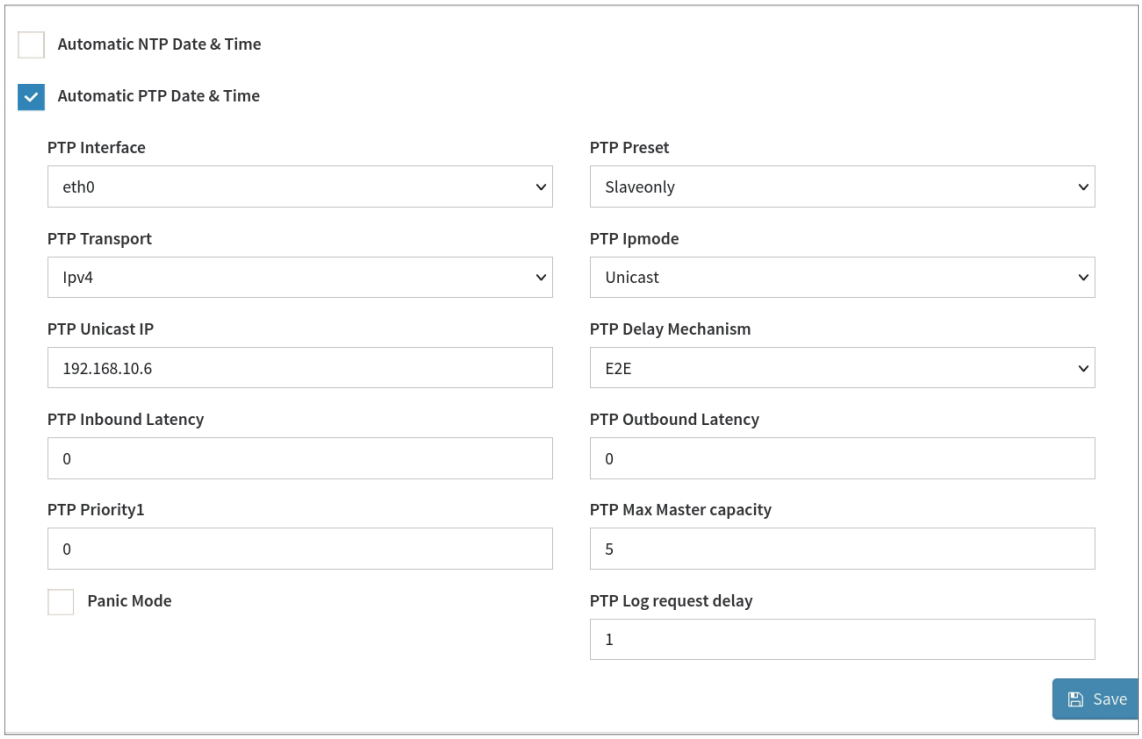
Navigate to the **Settings > Date & Time** page.

The user is able to configure the time zone as where he or she locates.

Additionally, by specifying the NTP server IP address, the BMC can synchronize its time and date with an external NTP server.



The user can also enable PTP to synchronize the BMC time with the master time server.

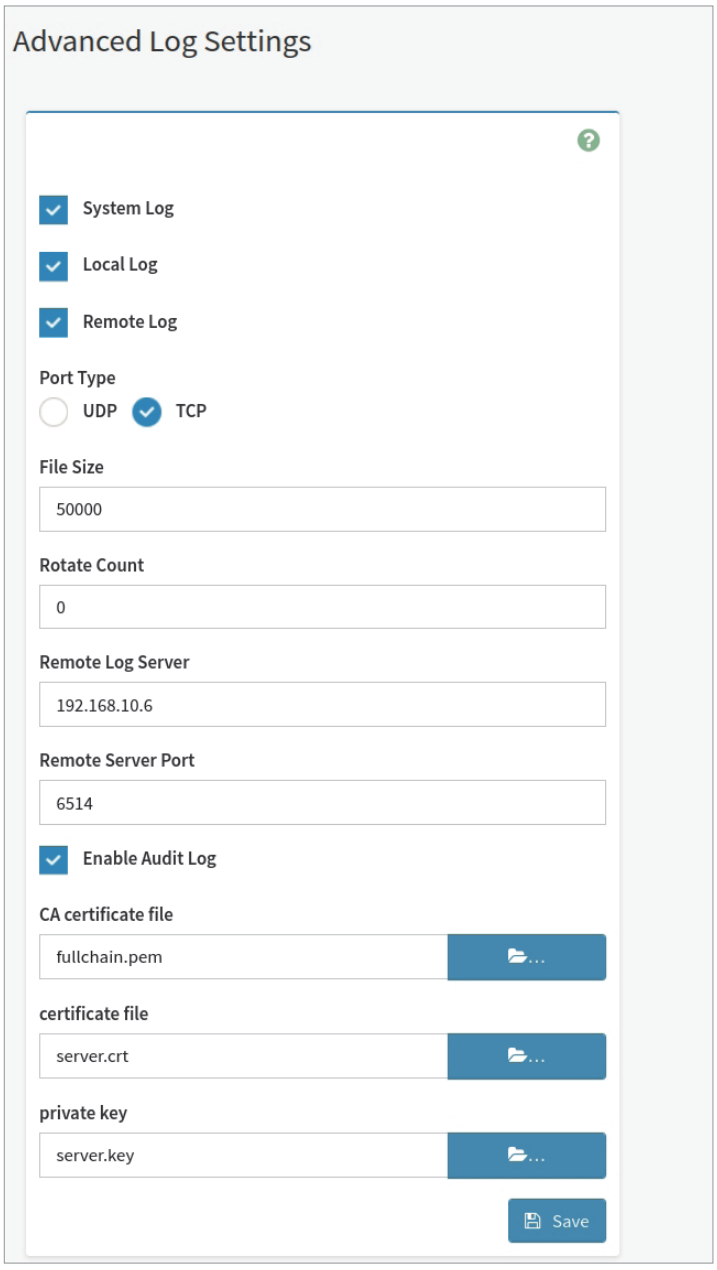


Note:
Only the PTP slave function is supported.

5.4.12 Remote Log

Navigate to the **Settings > Log Settings page > Advanced Log Settings** page. The user can configure remote logging to send syslog messages to a remote server.

The following figure shows remote logging in TCP mode. When TCP mode is selected, an authentication key is required.

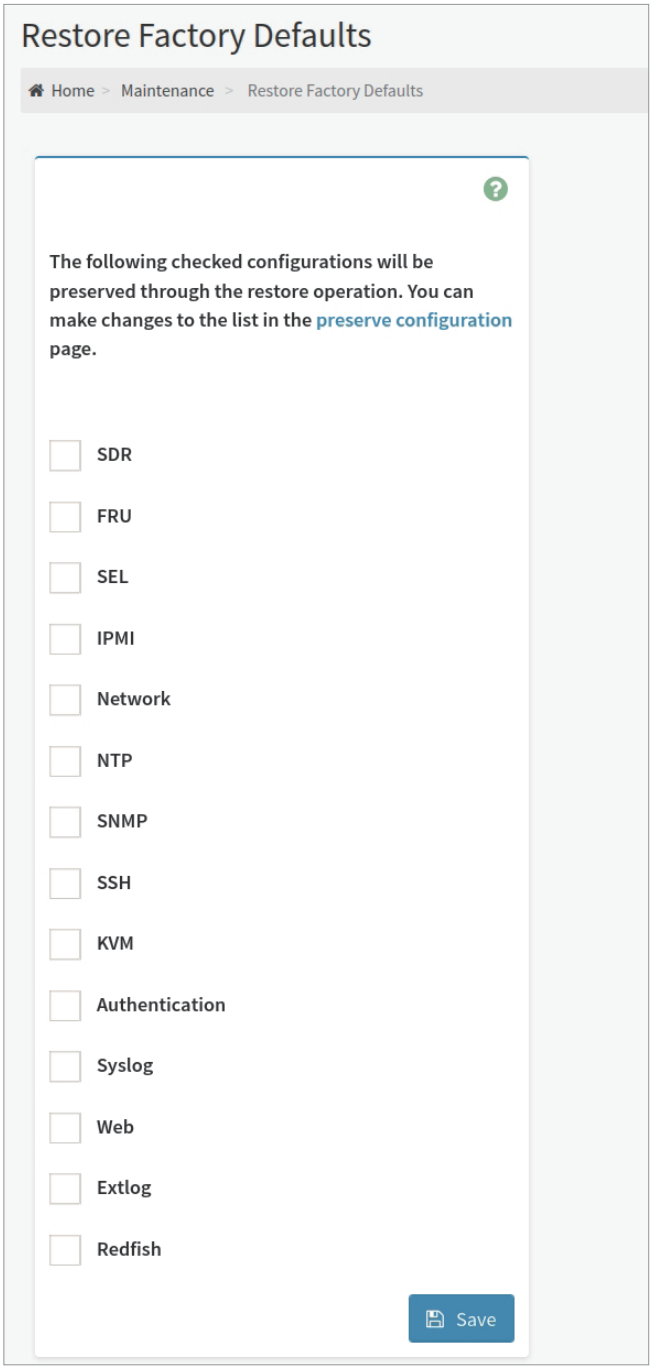


Note:
It is recommended to use rsyslog as remote log server.

5.4.13 Restore Factory Defaults

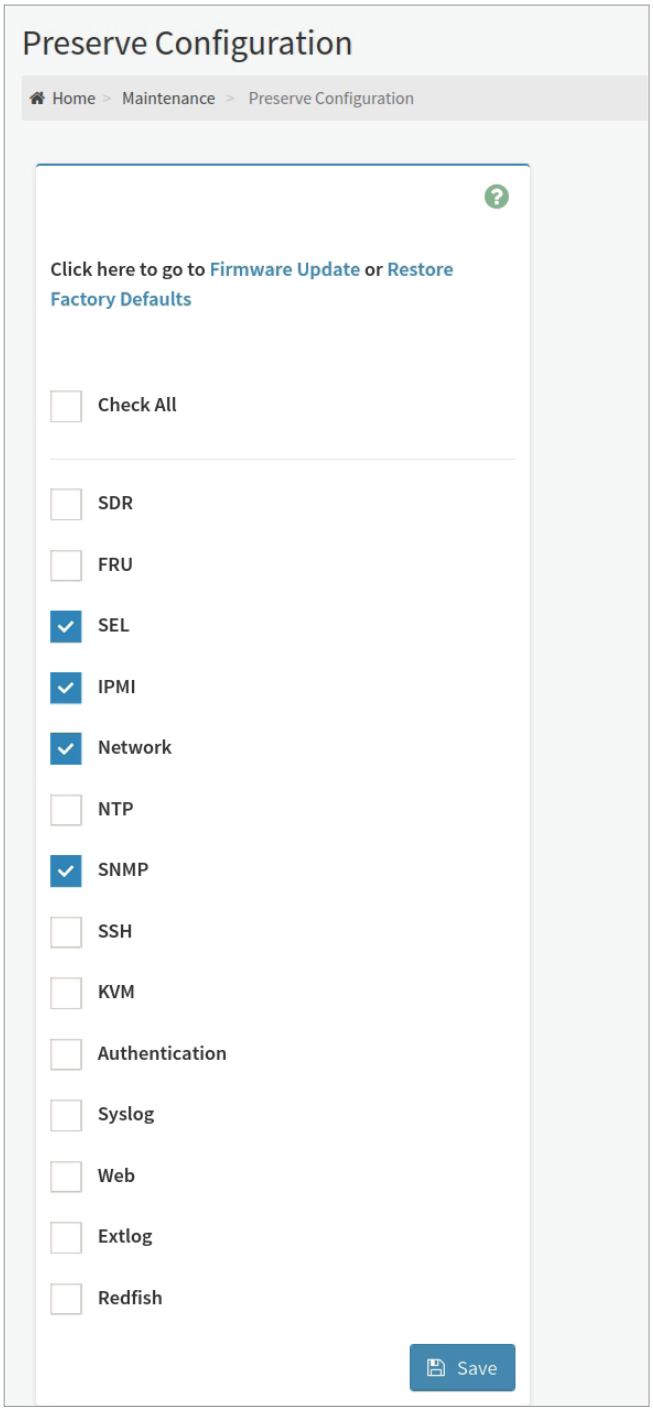
Navigate to the **Maintenance > Restore Factory Defaults** page.

The user can choose which configurations to restore to factory defaults. Note that the BMC firmware will reboot for the changes to take effect.



Note:
The user can pre-define which configurations to preserve during **BMC Firmware Update** and **Restore Factory Defaults**.

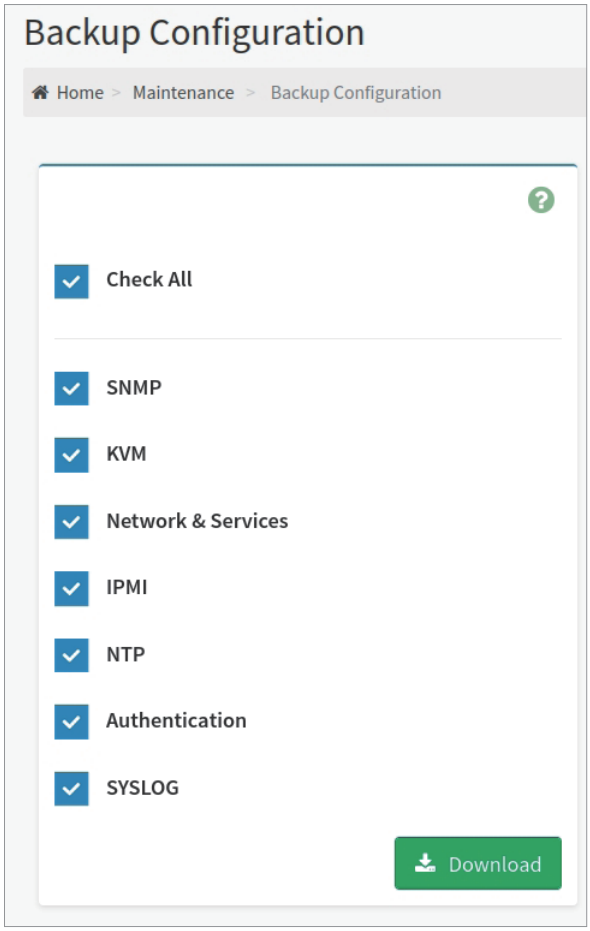
Navigate to the **Maintenance > Preserve Configuration** page.



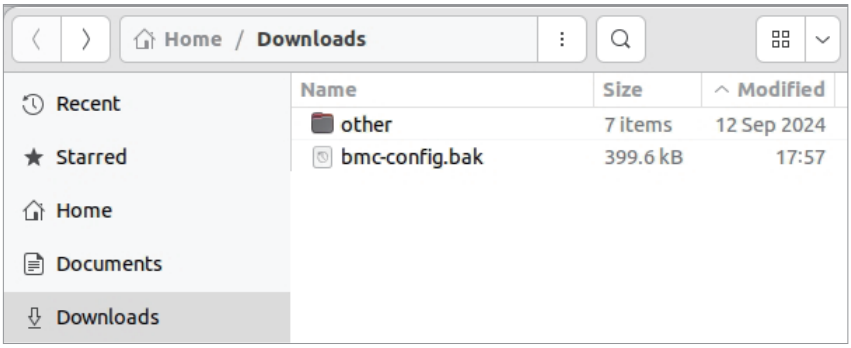
5.4.14 Backup Configuration

Navigate to the **Maintenance > Backup Configuration** page.

Select the configurations to backup, then click the “Download” button.



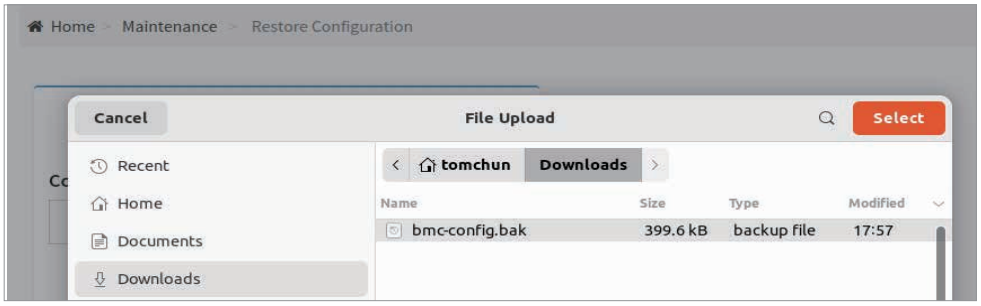
The following figure shows the BMC configuration backup file that can be used for restoration.



5.4.15 Restore Configuration

Navigate to the **Maintenance > Restore Configuration** page.

Select the BMC backup file to restore, then click the “Save” button.



The restore process will automatically reboot the BMC firmware to apply the new configuration.

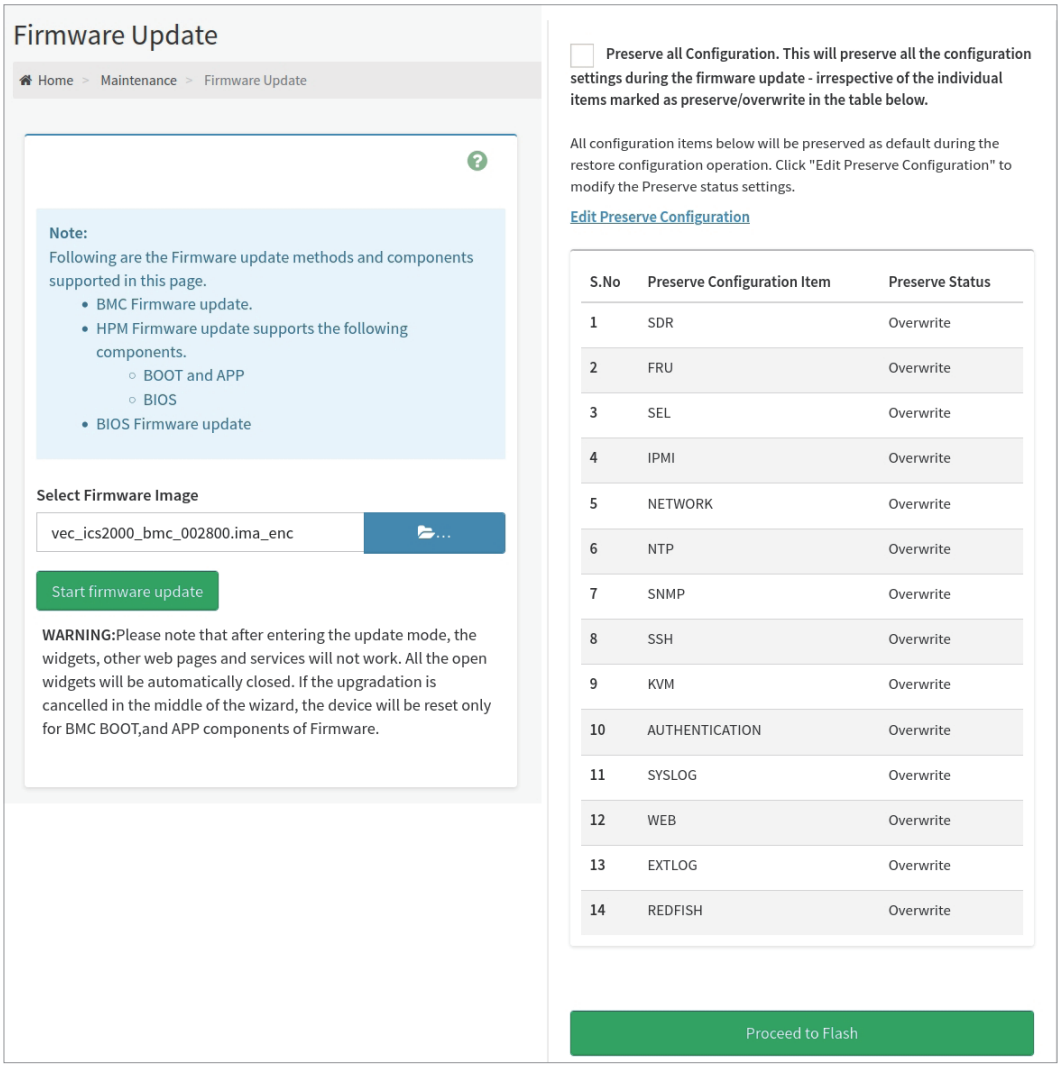
Note:
If IPMI configuration is restored, each user’s password will be restored to default.

5.4.16 Firmware Update

5.4.16.1 BMC Firmware Update

Navigate to the **Maintenance > Firmware Update** page.

Select the BMC firmware image to update, click the “Start firmware update” button to upload the image, and then click the “Proceed to Flash” button to begin the update process.

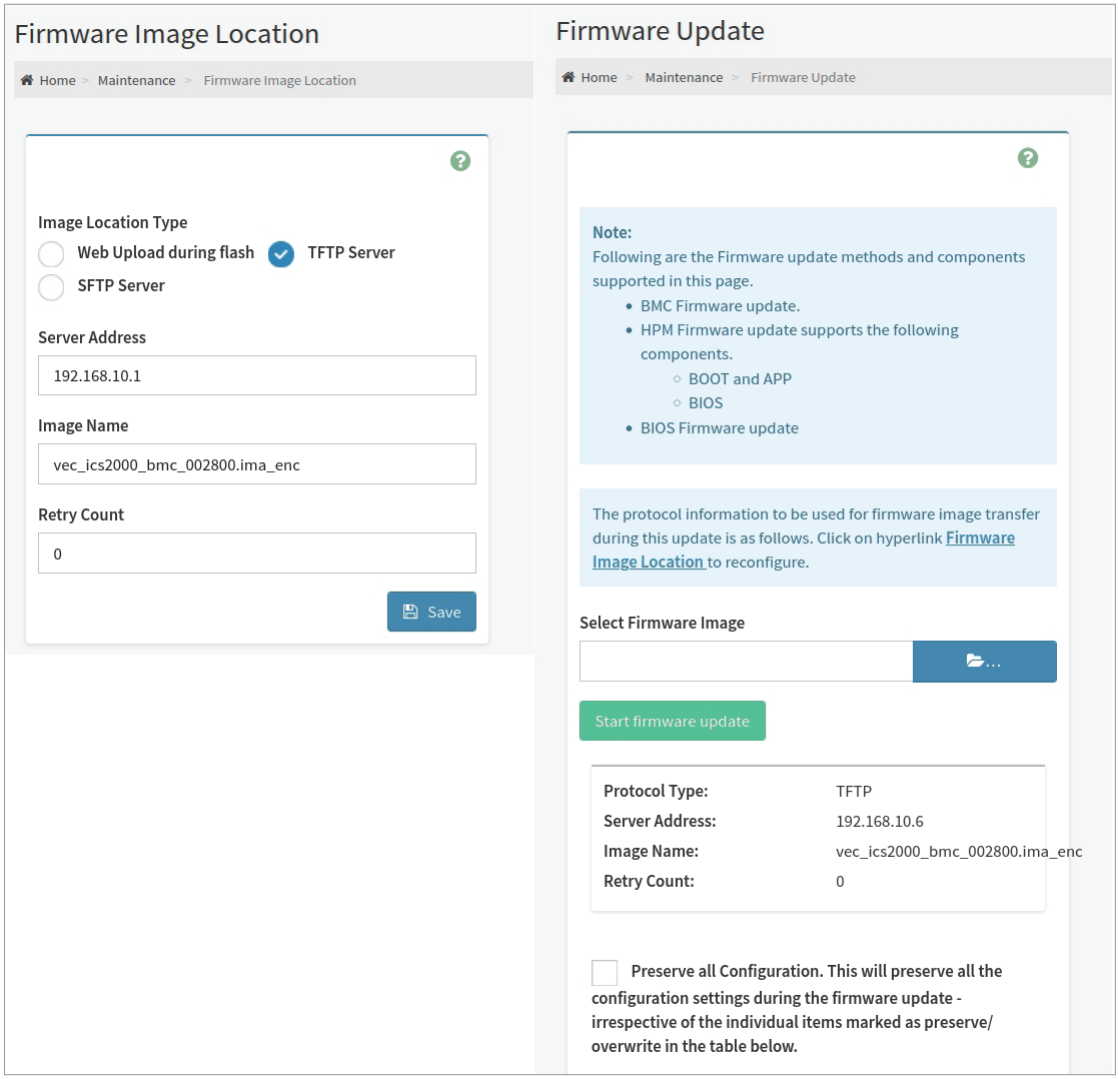


Alternatively, the BMC firmware image can be placed on a remote TFTP or SFTP server for downloading, instead of uploading it locally.

Navigate to the **Maintenance > Firmware Image Location** page.

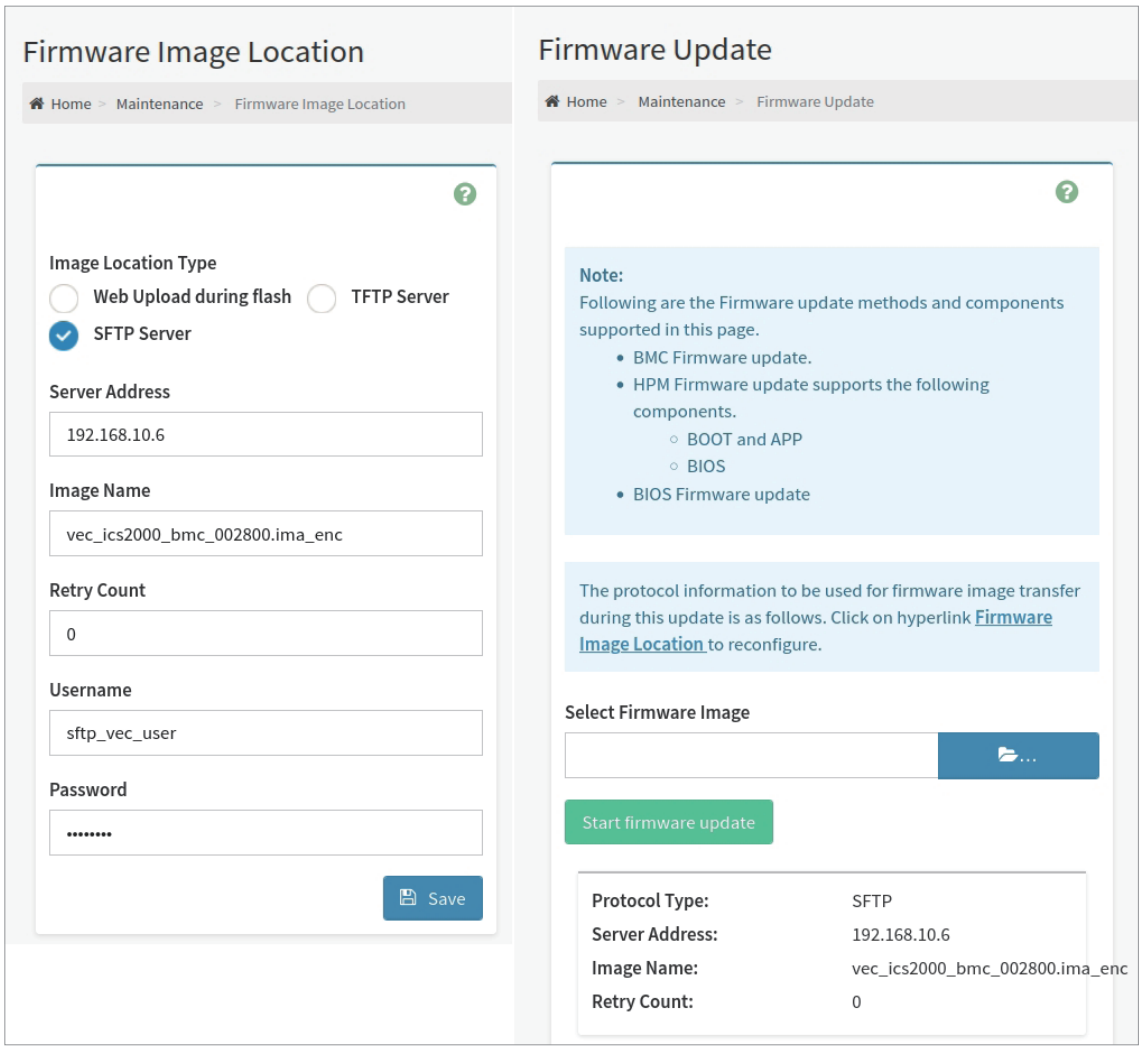
Configure the TFTP server address and specify the BMC firmware image file name.

Then, initiate the firmware update process by clicking the “Start firmware update” button.
No need to manually select the image file.



Alternatively, configure the SFTP server address and specify the BMC firmware image file name, retry count, username and password. Then, initiate the firmware update process.

The following figure illustrates the SFTP configuration, and BMC firmware update process.

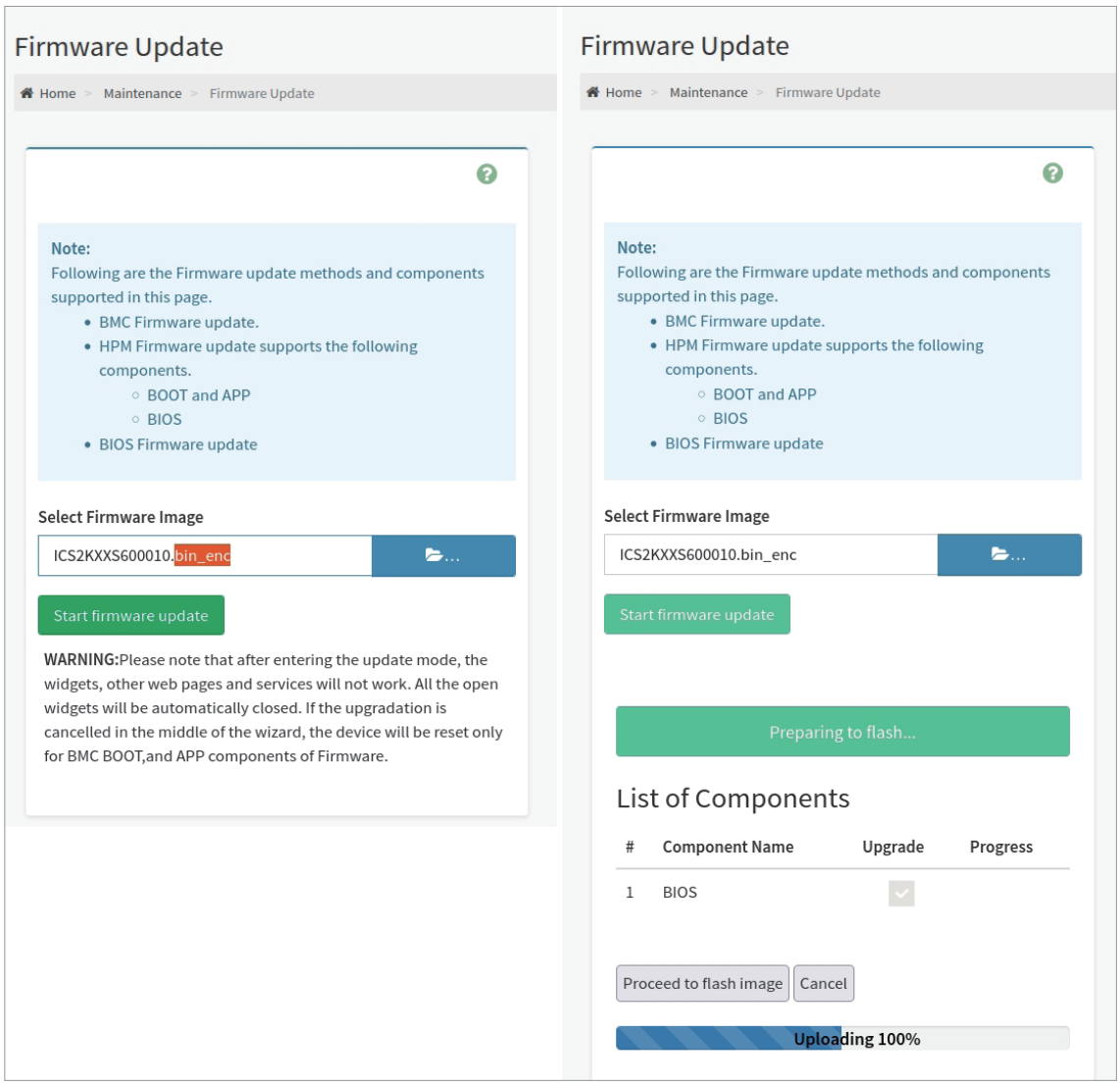


5.4.16.2 BIOS Firmware Update

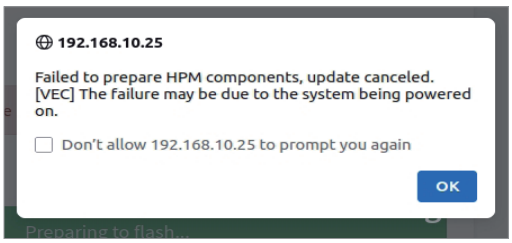
Navigate to the **Maintenance > Firmware Update** page.

Select the BIOS firmware image to update, click the “Start firmware update” button to upload the image, and then click the “Proceed to flash image” button to begin the update process.

After the firmware update is complete, the system will power on automatically.

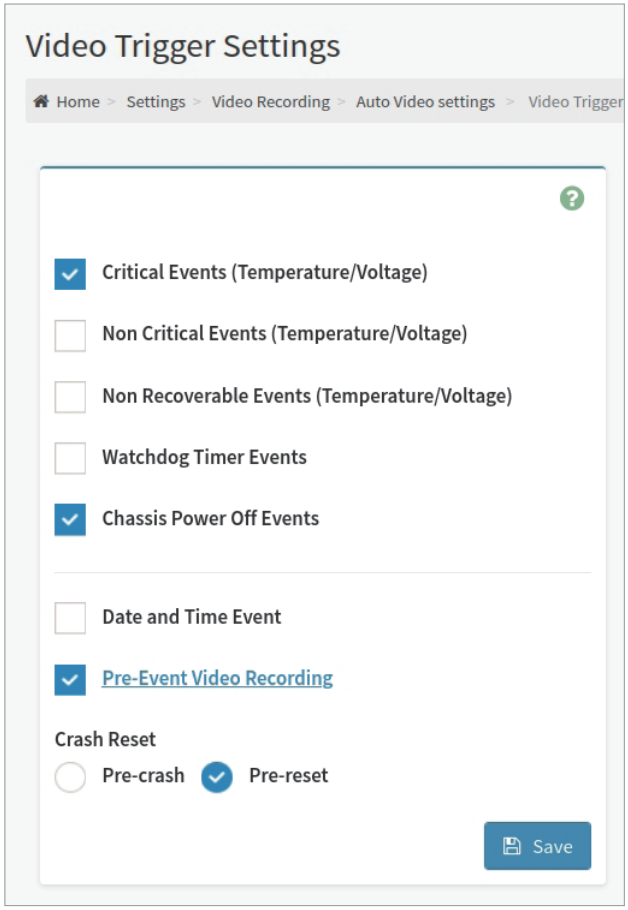


Note:
BIOS firmware updates are only permitted when the host is powered off to prevent unexpected issues.



5.4.17 Video Record

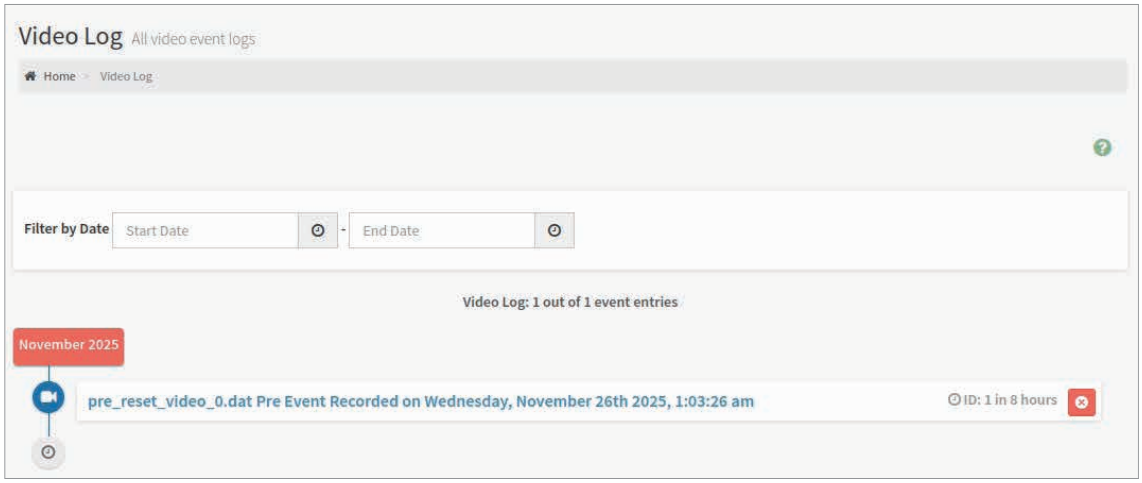
Navigate to the **Settings > Video Recording > Auto Video settings > Video Trigger Settings** page.



Enable Pre-Event Video Recording and select the 'Pre-reset' option. Then, reset the system to initiate video recording.

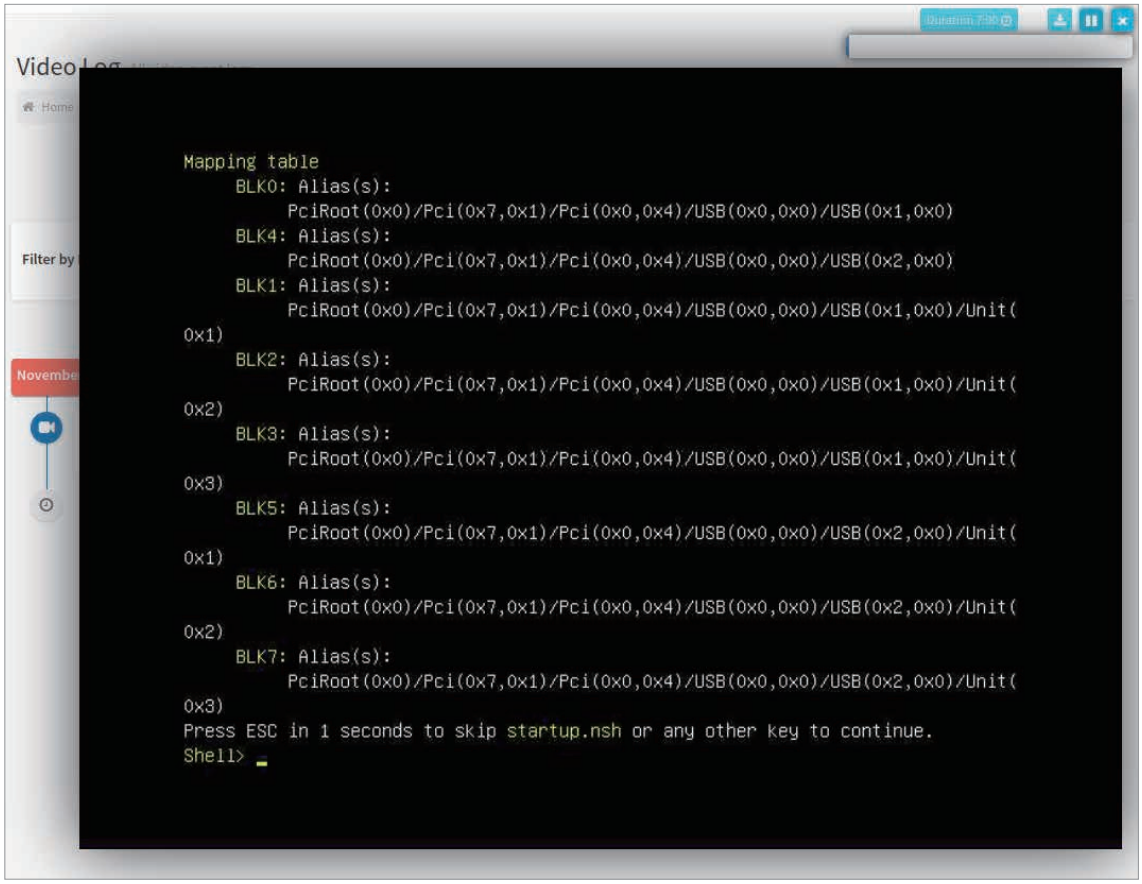
Navigate to the **Logs & Reports > Video Log** page.

The following figure illustrates the pre recorded video trigger by reset event.



To play the vedio, click the link the play the video directly on HTML5 WebUI.

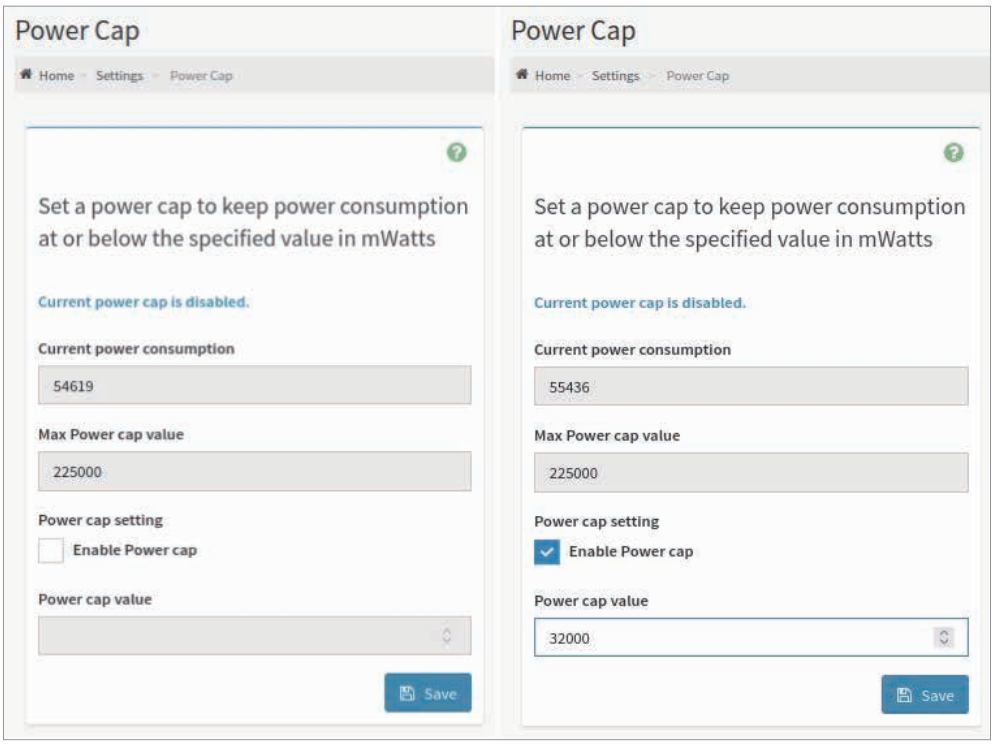
The following figure illustrates a snapshot of the video playing.



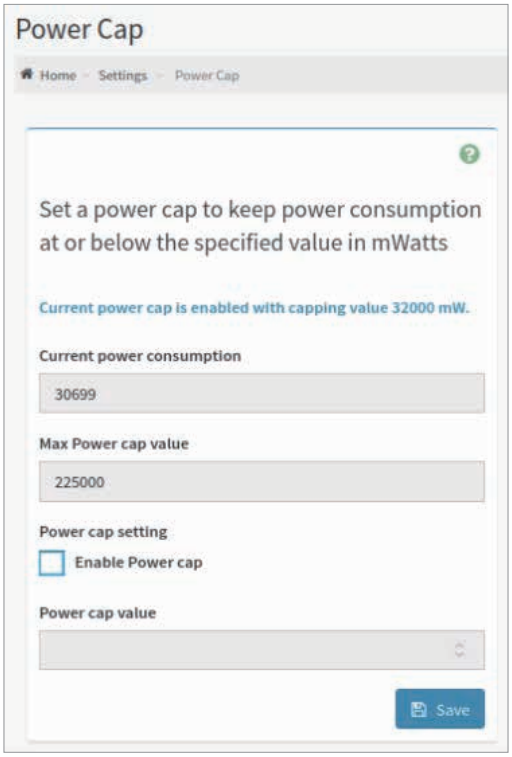
5.4.18 Power Cap

Navigate to the **Settings > Power Cap** page.

The feature allows limiting AMD CPU power consumption.
The power cap can only be configured after the BIOS has completed its boot process.



The following figure indicates the Power Cap settings and its result.



5.5 Redfish Management

The VECOW BMC firmware is compliant with Redfish version 1.15.1 and schema version 1.0.19

5.5.1 Getting Started

The POSTMAN application is commonly used for Redfish-based communication.

VECOW provides a standard POSTMAN collection that includes commonly used Redfish APIs for ease of use and quick access.

Note:
This documentation uses POSTMAN to demonstrate Redfish API requests. However, customers may use alternative tools such as cURL if preferred. For additional guidance, please contact VECOW.

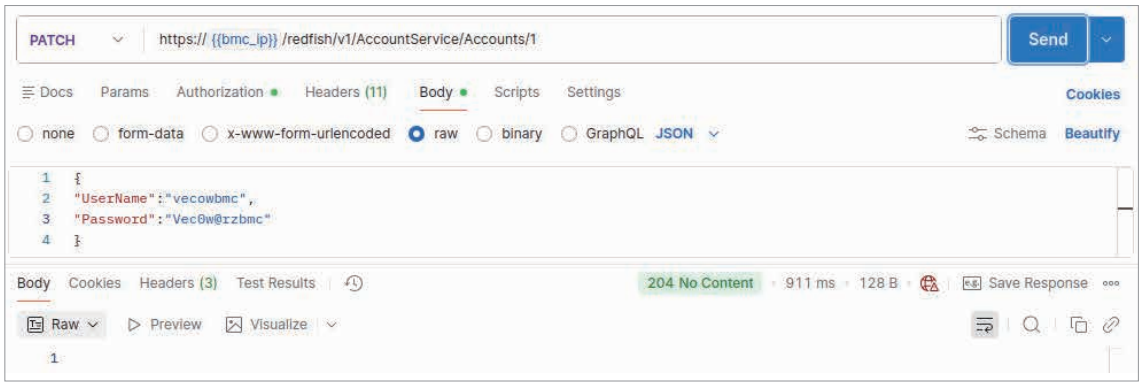
5.5.1.1 VECOW Redfish Default Credentials

Username: **Administrator**
Password: **superuser**

Redfish credentials are NOT shared with the BMC Web UI or IPMI, meaning they are managed separately and are independent of IPMI user accounts.

The default Redfish credentials cannot be used directly for Redfish authentication. Before using Redfish, the default Redfish username and password MUST be changed.

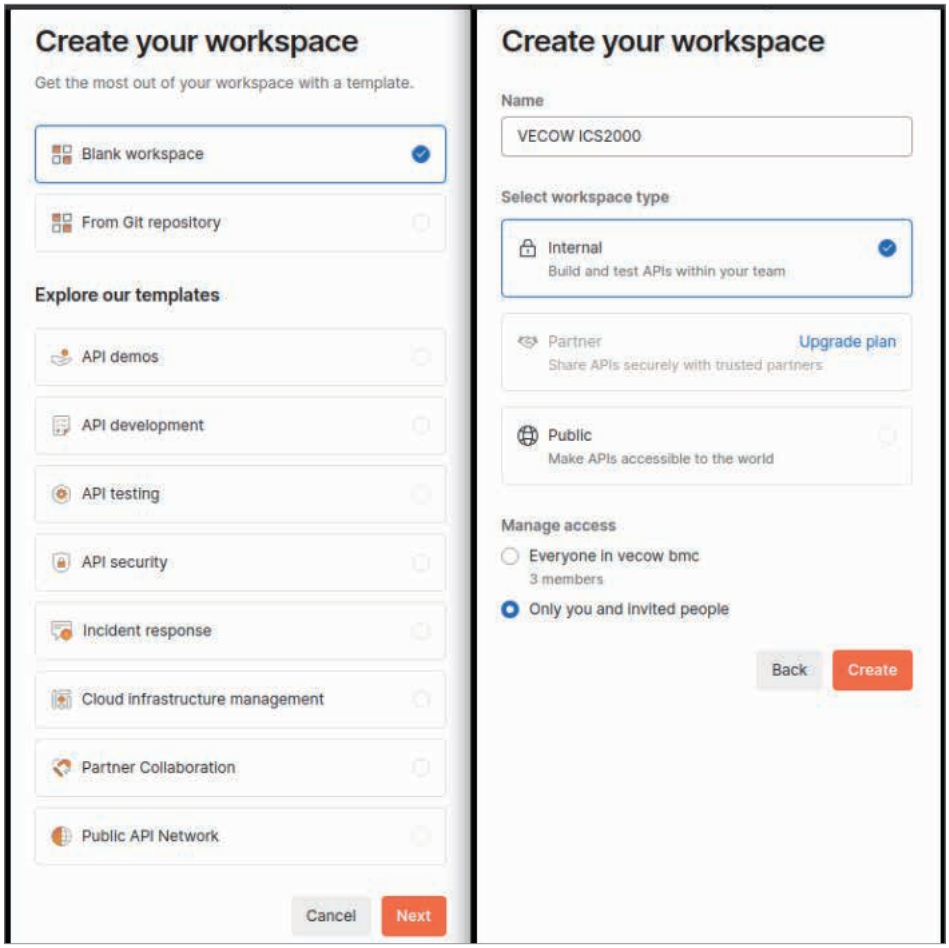
The following figure illustrates how to use POSTMAN to modify the default credentials.



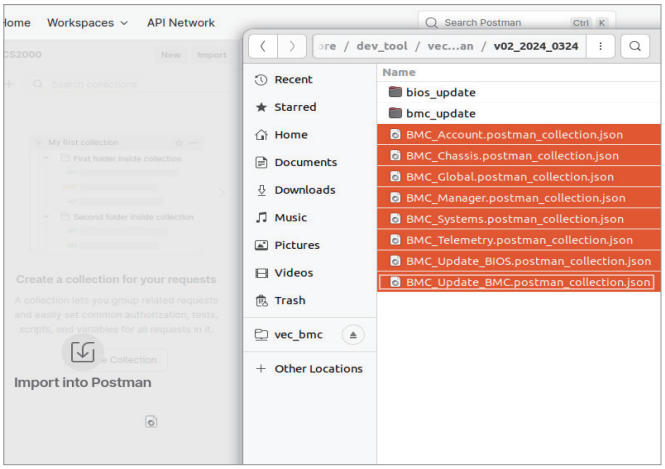
Note:
The Redfish credentials will reset to default, after updating the BMC firmware or restoring the BMC to its factory default. Therefore, the Redfish credentials must be modified again.

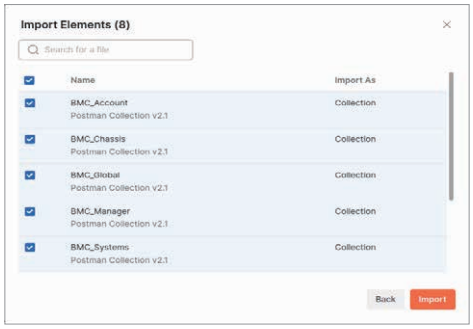
5.5.1.2 VECOW POSTMAN Redfish Collection Import

The following figure illustrates how to create a POSTMAN workspace specific to the project and import the VECOW Redfish API collection into workspace.

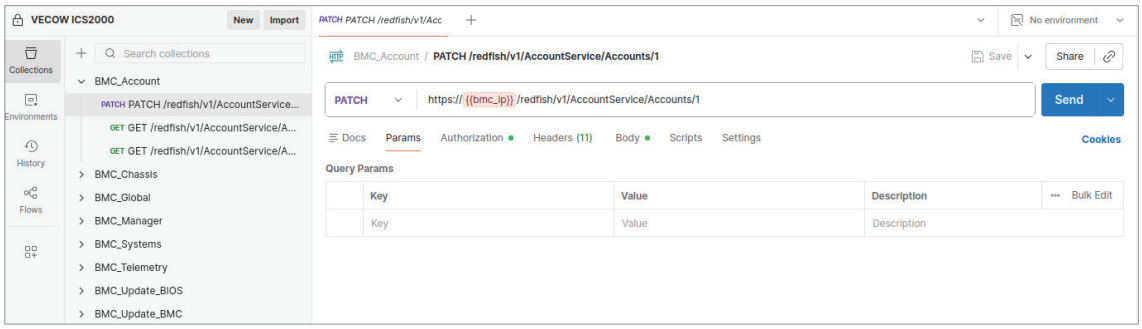


Drag the VECOW Redfish API collection JSON files into the project-specific workspace.



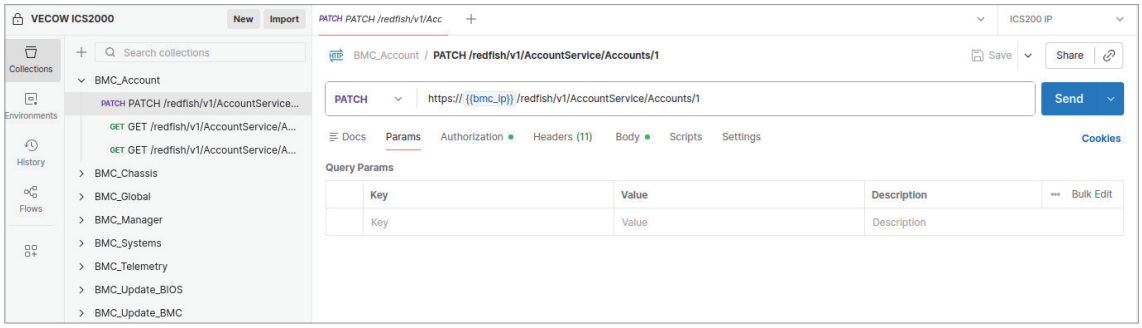


The following figure illustrates the imported VECOW Redfish API collection.



After importing the collection, configure the POSTMAN environment variable with the desired IPv4 or IPv6 address to further simplify the use of Redfish APIs.

This allows the IP address to be applied across all Redfish API requests in the POSTMAN collection, eliminating the need to update the IP address in each individual request.



Please create an environment variable named *bmc_ip*, set its value to the actual BMC IP address, and assign this environment to the workspace.

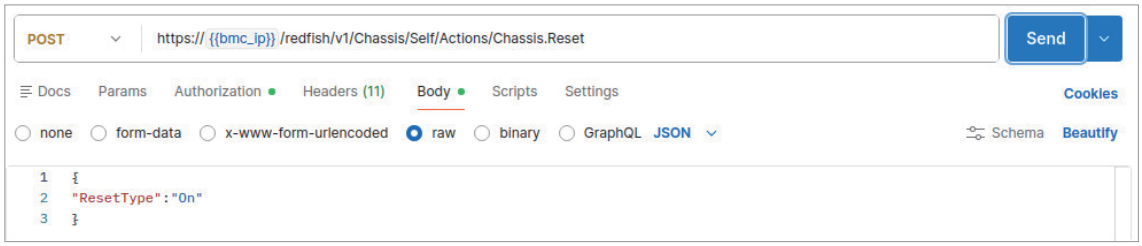


5.5.2 Chassis Power Control

The chassis control actions that can be specified in the request body include:

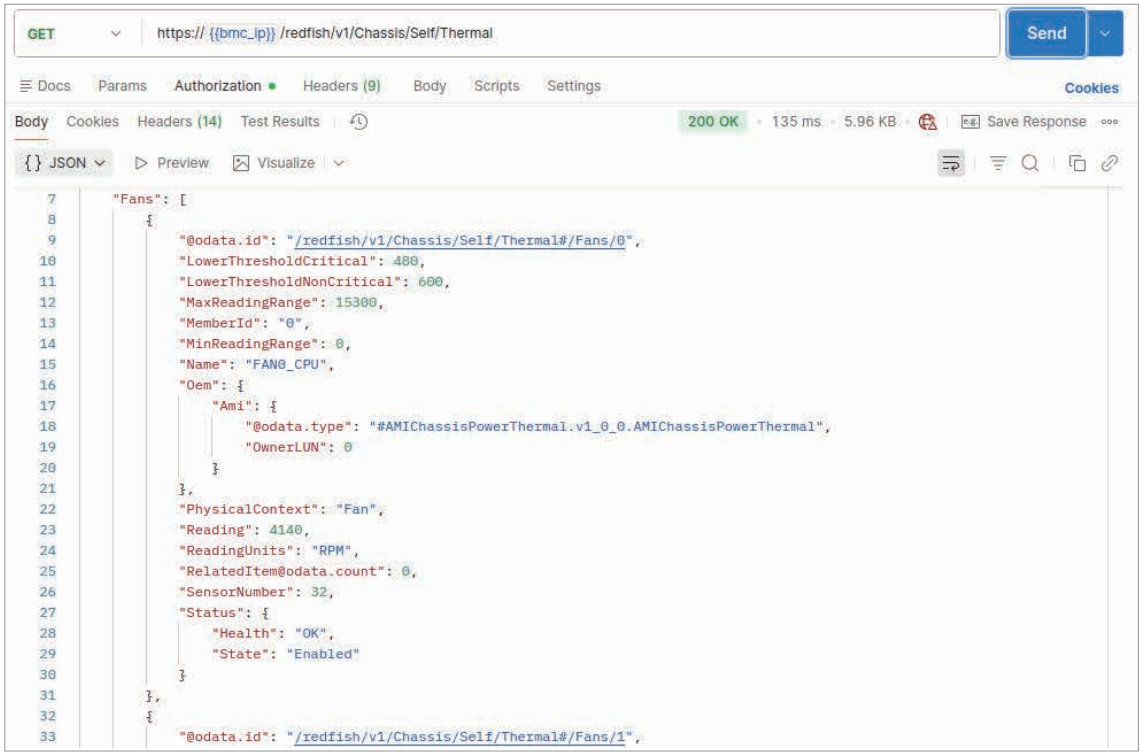
"ResetType":"On"
"ResetType":"ForceOff"
"ResetType":"GracefulShutdown"
"ResetType":"PowerCycle"
"ResetType":"ForceRestart"

The following figure illustrates chassis power on request.

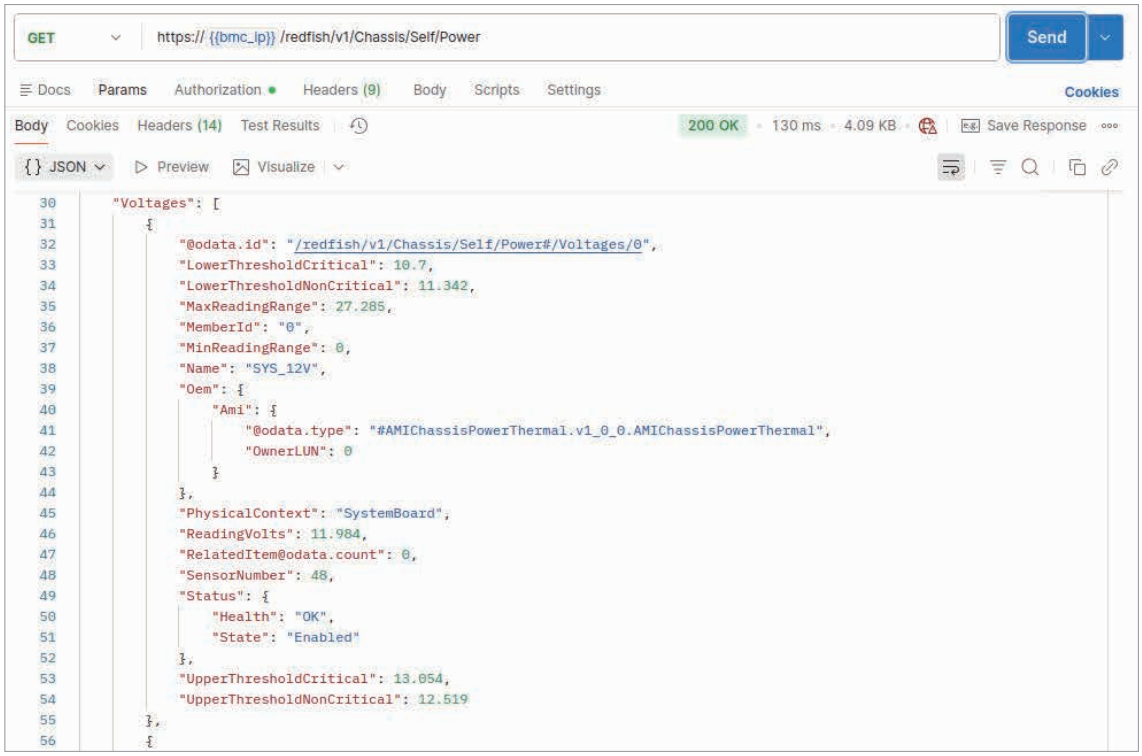


5.5.3 Redfish Sensor Monitoring

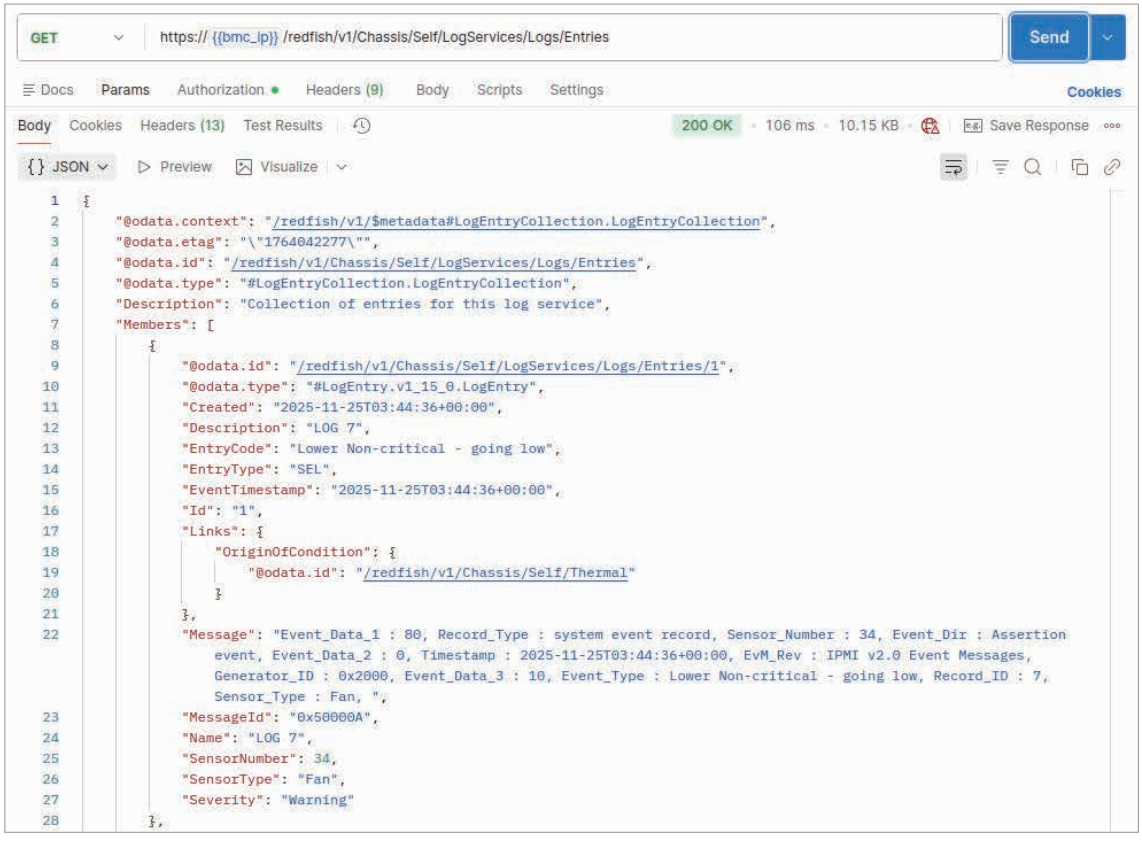
The following figure illustrates how to retrieve the thermal sensors.



The following figure illustrates how to retrieve the power sensors.

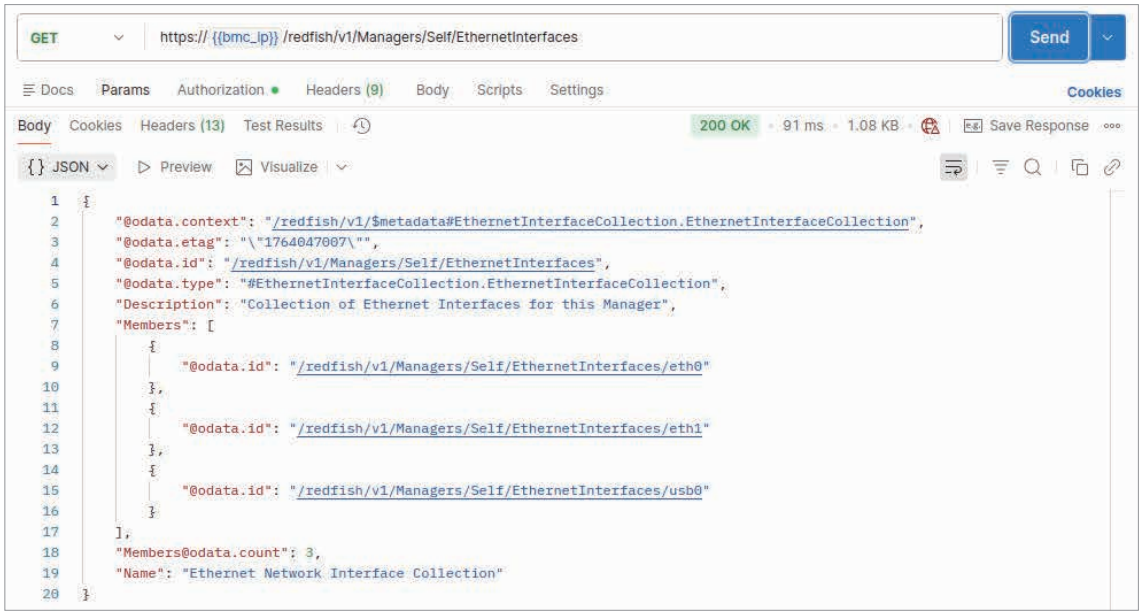


The following figure illustrates how to retrieve the sensor log entries.

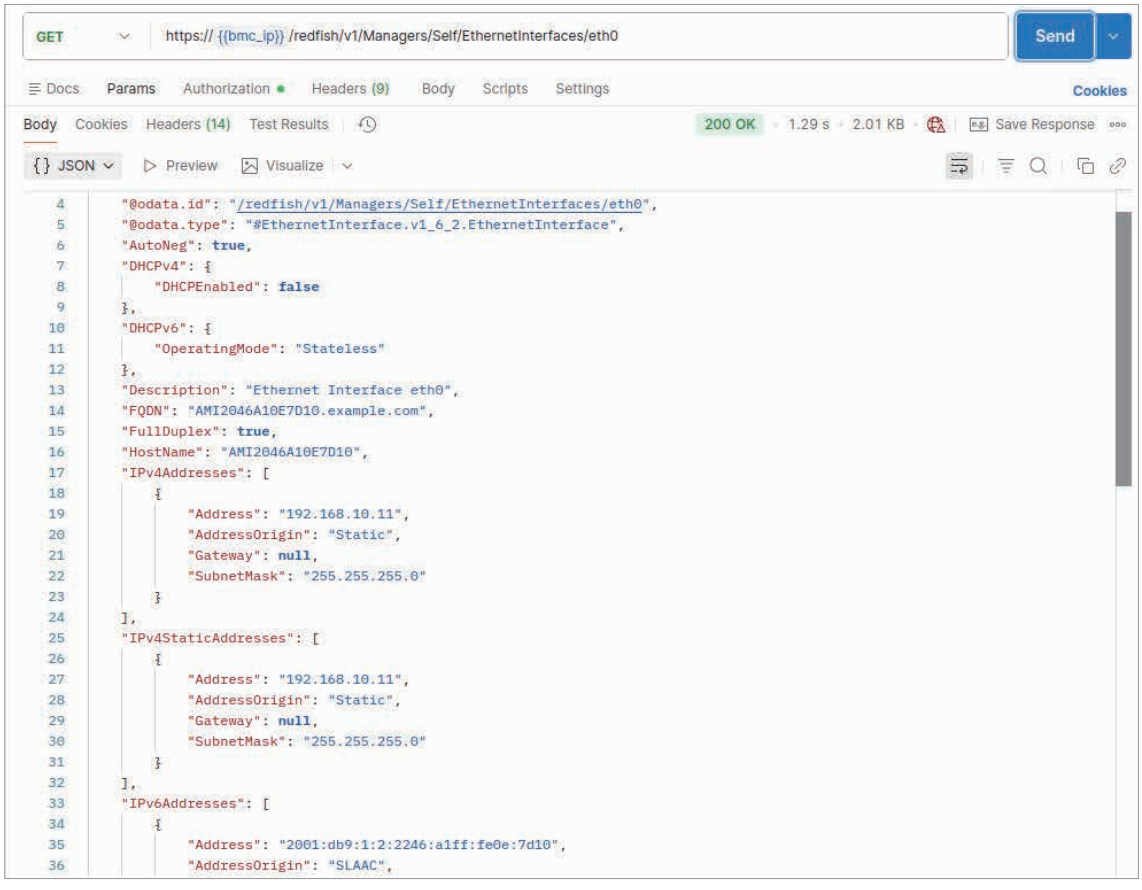


5.5.4 Network Configuration

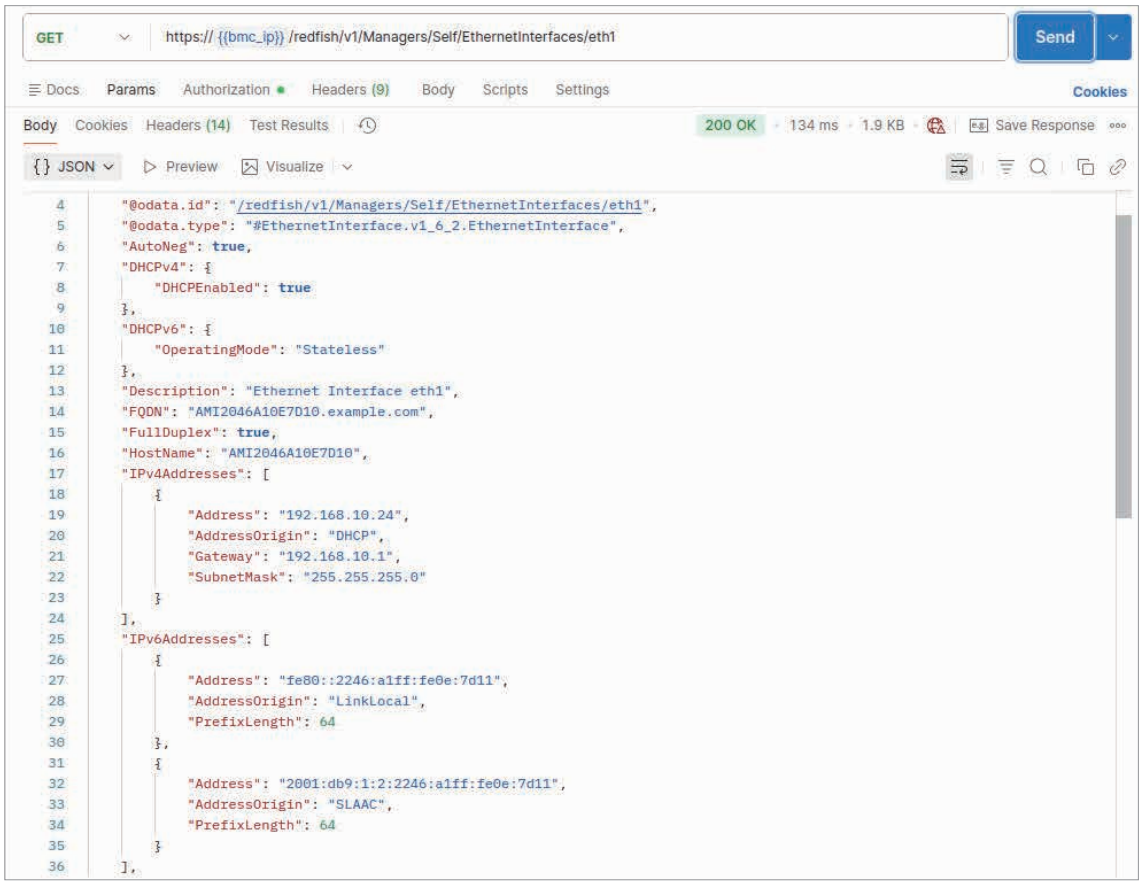
The following figure illustrates how to retrieve the available LAN interfaces of the BMC firmware.



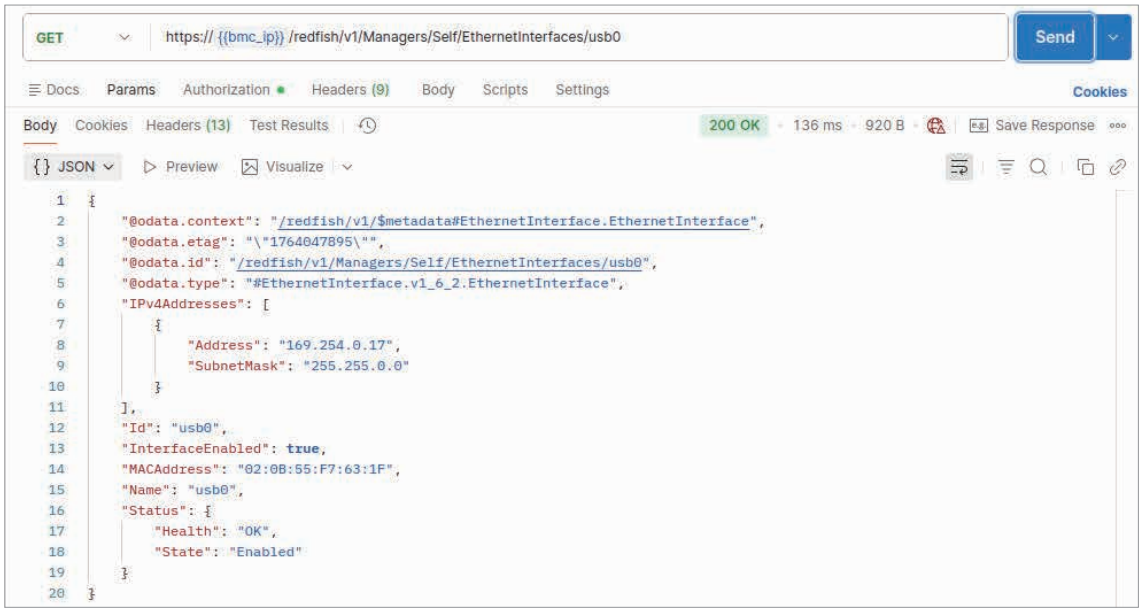
The following figure illustrates how to retrieve network information for eth0 (the dedicated NIC).



The following figure illustrates how to retrieve network information for eth1 (the shared NIC).



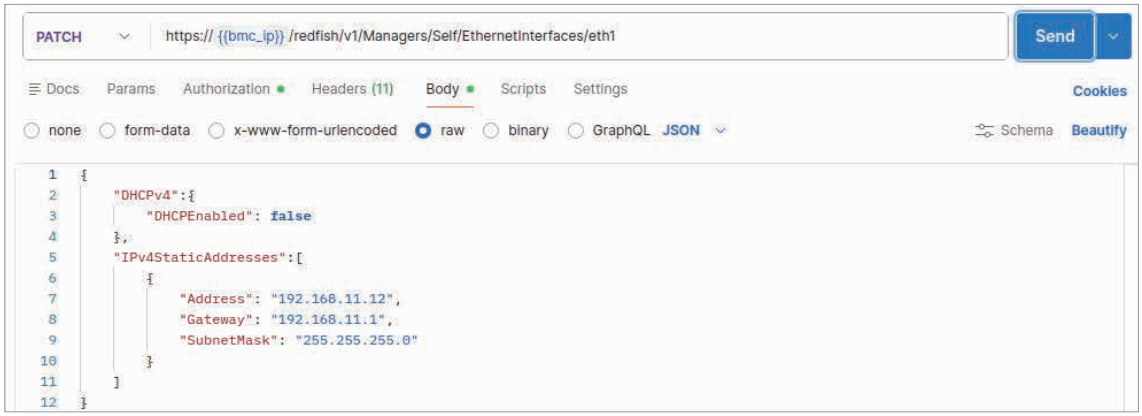
The following figure illustrates how to retrieve network information for usb0 (the USB over LAN).



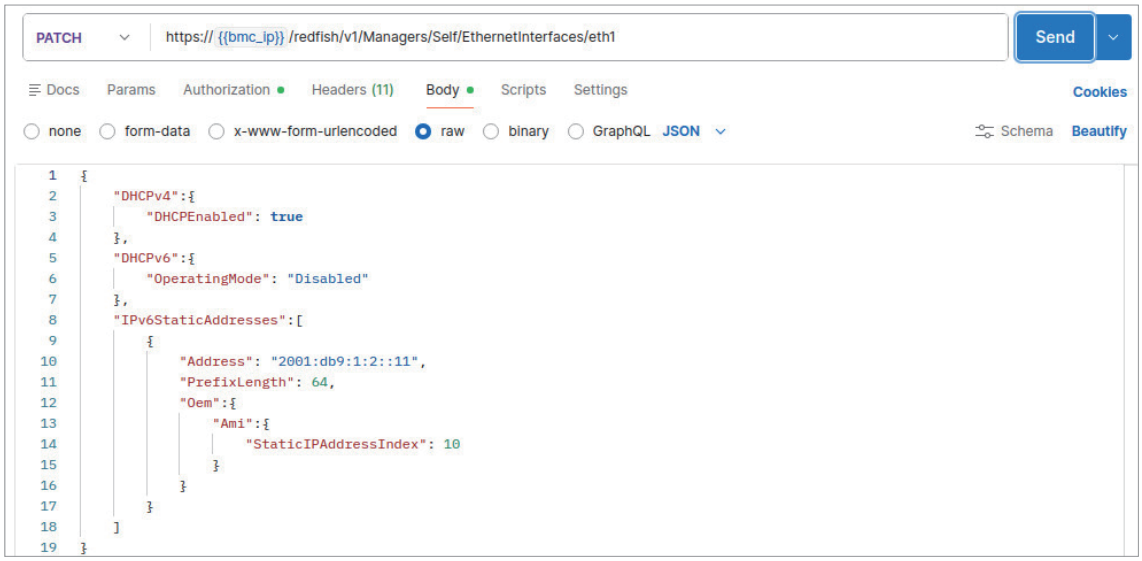
The following figure illustrates how to modify the IPv4 static address of the dedicated NIC.



The following figure illustrates how to modify the IPv4 DHCP mode, and IPv4 static address of the shared NIC.



The following figure illustrates how to modify the IPv4 DHCP mode, and IPv6 static address of the shared NIC.



5.5.5 Firmware Update

5.5.5.1 BMC Firmware Update

Navigate to upload three files, including BMC firmware image file, and two parameter json files.

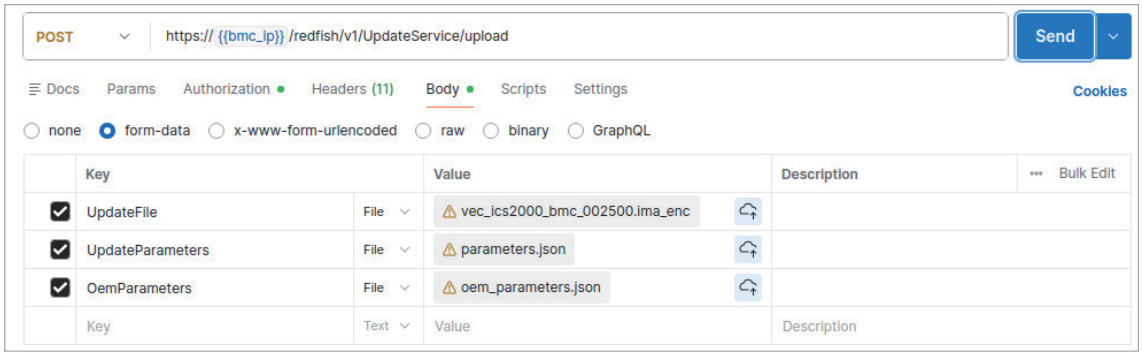
Content of **UpdateParameters** json file is as follows:

```
{
  "Targets": [
    "/redfish/v1/UpdateService/FirmwareInventory/BMC"
  ]
}
```

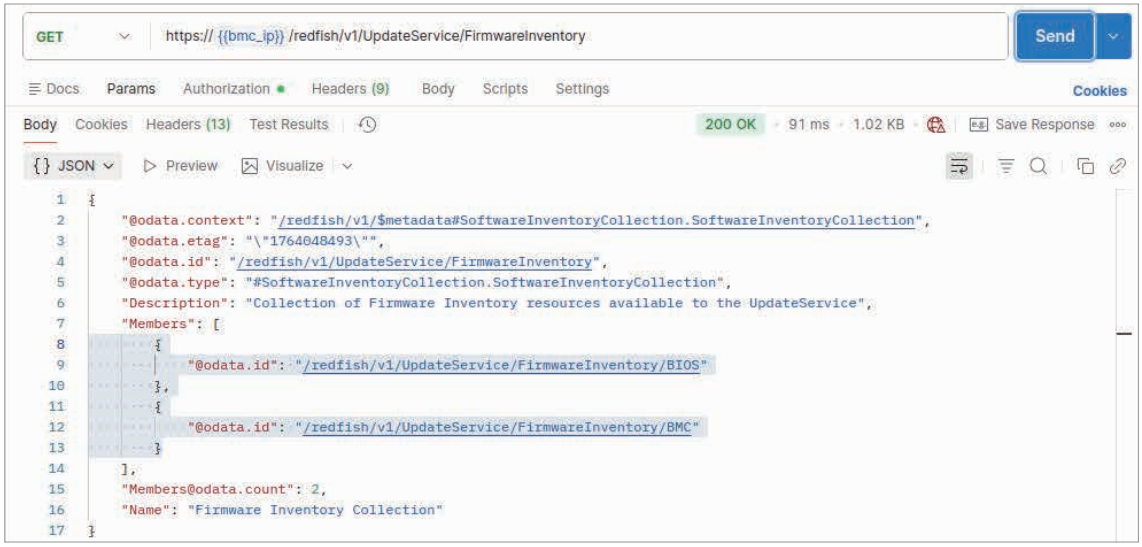
*Content of **OemParameters** json file is as follows:*

```
{
  "ImageType": "BMC"
}
```

The following figure illustrates the configuration settings for the BMC firmware update.



Note:
If the BMC or BIOS firmware update fails, the user can verify if the firmware update option is available.



5.5.5.2 BIOS Firmware Update

Navigate to upload three files, including BIOS firmware image file, and two parameter json files.

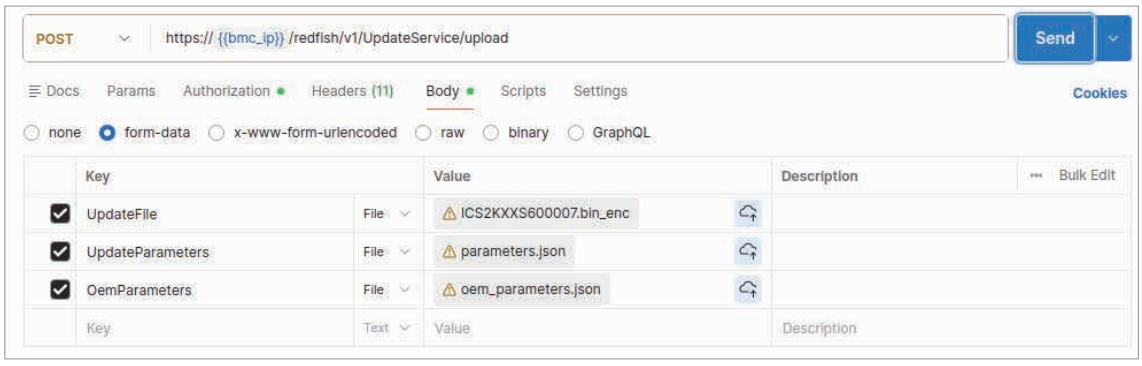
Content of **UpdateParameters** json file is as follows:

```
{
  "Targets": [
    "/redfish/v1/UpdateService/FirmwareInventory/BIOS"
  ]
}
```

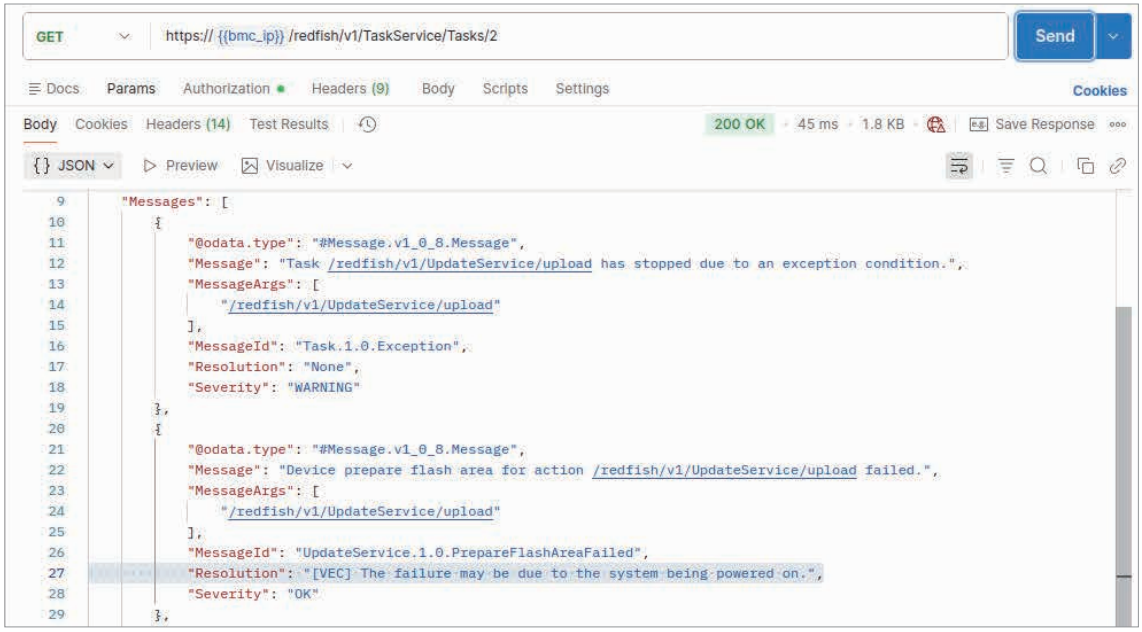
*Content of **OemParameters** json file is as follows:*

```
{
  "ImageType": "BIOS"
}
```

The following figure illustrates the configuration settings for the BIOS firmware update.

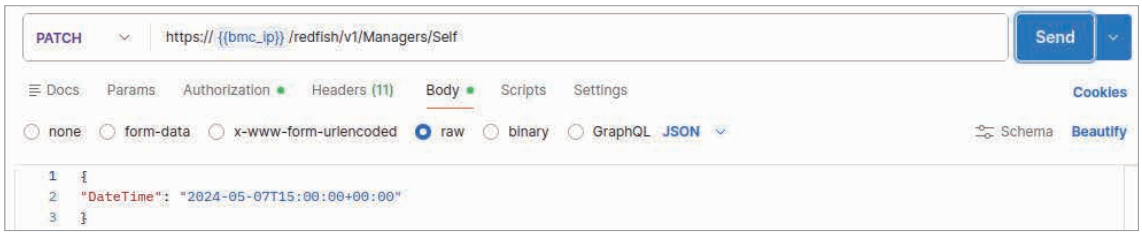


Note:
BIOS firmware updates are only permitted when the host is powered off to prevent unexpected issues.



5.5.6 Date and Time Configuration

The following figure illustrates how to update the data and time via the Redfish API.

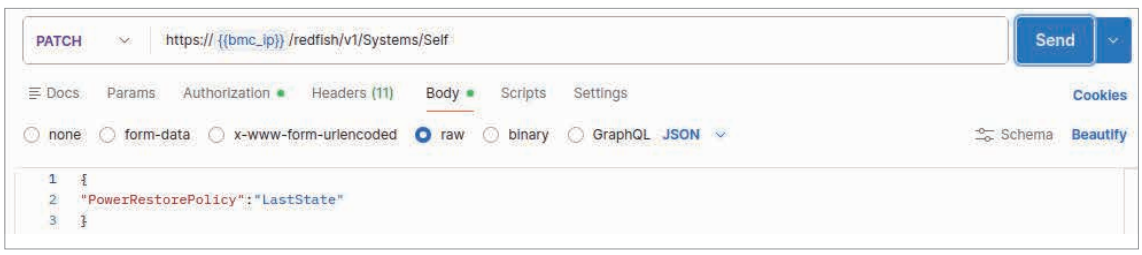


5.5.7 Power Restore Policy Configuration

The power restore policy that can be specified in the request body include:

"PowerRestorePolicy":"AlwaysOn"
"PowerRestorePolicy":"AlwaysOff"
"PowerRestorePolicy":"LastState"

The following figure illustrates how to modify the power restore policy via the Redfish API.



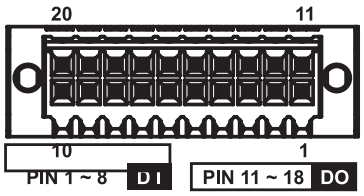
APPENDIX A : Isolated DIO Guide

A.1 Function Description

The ICS-2000 offers one 16-bit Isolated DIO 20-pin terminal block connector, and a 4-port serial interface; each of the four serial ports can be configured as RS-232, RS-422, or RS-485.

Isolated DIO pins are fix by Hardware design that cannot change in/out direction in runtime process.

DIO definition is shown below :

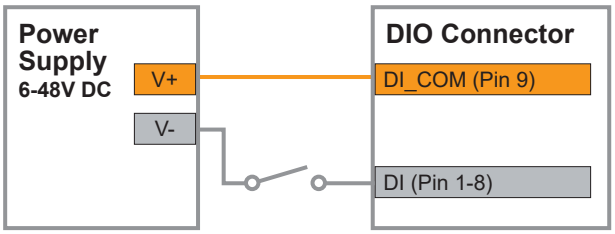


Pin No.	Isolated DIO	Non-Isolated DIO Definition	Pin No.	Isolated DIO Definition	Non-Isolated DIO Definition
1	DI 0	DIO 0	11	DO 0	DIO 8
2	DI 1	DIO 1	12	DO 1	DIO 9
3	DI 2	DIO 2	13	DO 2	DIO 10
4	DI 3	DIO 3	14	DO 3	DIO 11
5	DI 4	DIO 4	15	DO 4	DIO 12
6	DI 5	DIO 5	16	DO 5	DIO 13
7	DI 6	DIO 6	17	DO 6	DIO 14
8	DI 7	DIO 7	18	DO 7	DIO 15
9	DI COM	NC	19	DIO_GND	DIO_GND
10	DIO_GND	DIO_GND	20	External VDC	NC

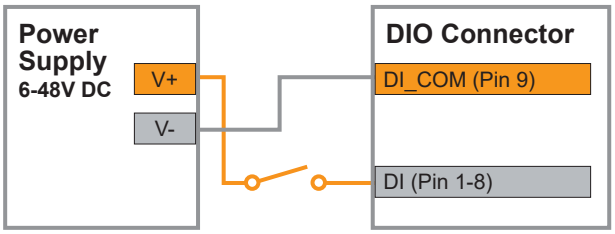
A.2 Isolated DIO Signal Circuit

DI reference circuit :

Sink Mode
(NPN)

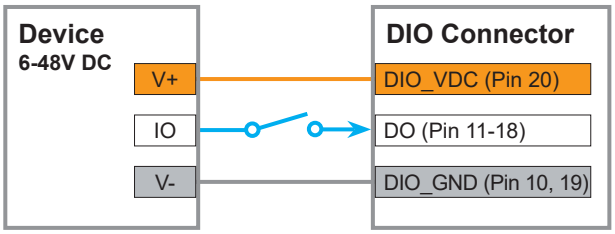


Source Mode
(PNP)

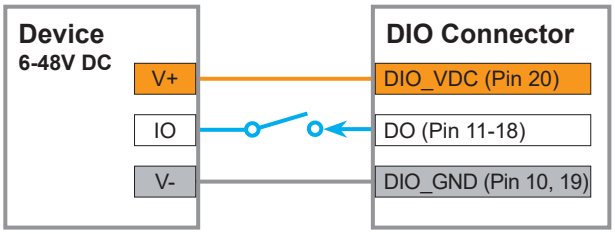


DO reference circuit :

Sink Mode
(NPN, Default)



Source Mode
(PNP)

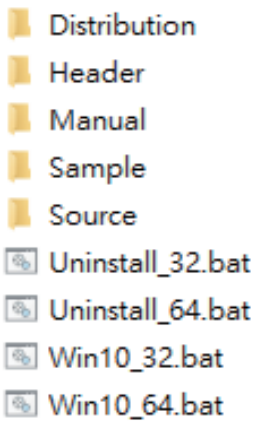


A.3 Software Package Contain

- Distribution folder include x32 and x64 versions, use batch file for installation.
  There are included as fallowed :
    Win10_32.bat, and Win10_64.bat :
      Installation for driver, and
    Uninstall_32.bat, and Uninstall_64.bat :
      Uninstallation for driver
  Run batch file as Administrator.

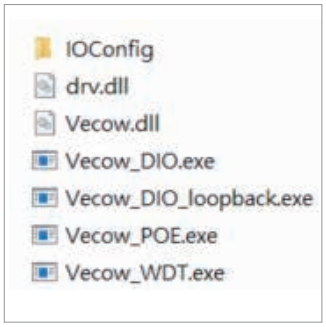
Make sure Windows version before installation.

- Header folder include head file for software developer or System Integration.
- Manual folder include API description.
- Sample folder include sample program, driver library, and API library for Windows/Linux
- Source folder include sample program source code that compile on Visual Studio 2008/Ubuntu18.04.

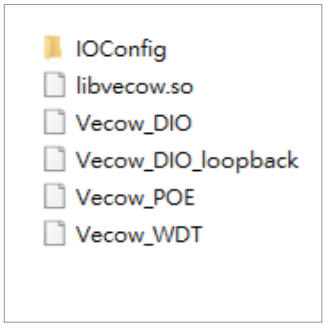


A.4 Sample

Execute demo tool.



Windows



Linux

Sample, as shown below :

```
DIO sample version : v1.0.0609.0608
Load Vecow.dll at least v1.8.1409.0608
Vecow.dll Version : v1.8.1409.0608
Config : IO port  I - Isolated DIO
         IO port II - Non-Isolated DIO(GPIO)

Choose IO : (1/2)
```

Vecow_DIO

```
DIO loopback sample version : v1.0.1509.0608
Load Vecow.dll at least v1.8.1409.0608
Vecow.dll Version : v1.8.1409.0608
Config : IO port  I - Isolated DIO
         IO port II - Non-Isolated DIO(GPIO)

How many IO temp_port : (1/2)
```

Vecow_DIO_loopback

```
COMPORT sample version : v1.0.0309.0608
Load Vecow.dll at least v1.8.1409.0608
Vecow.dll Version : v1.48.0701.0000
PCB_ver = B

COMPORT1 mode : RS232
COMPORT2 mode : RS232
COMPORT3 mode : RS232
COMPORT4 mode : RS232
Choose port : (1~4) 1
COMPORT1 mode selection: 0:RS232
                         1:RS422-5W
                         2:RS422-9W
                         3:RS485
                         4:Loopback
Select port mode : 0
Set COMPORT mode success!
```

Vecow_COMPORT

B

APPENDIX B : Software Functions

B.1 Driver API Guide

In Header folder, Vecow.h and VecowLinux.h contain usabled API for Windows/Linux.

BOOL initial_SIO(BYTE Isolate_Type, BYTE DIO_NPN)
Initial machine for IO and watch dogtimer.
Isolate_Type : DIO type.
1 : Isolated DIO;
0 : Non-Isolated DIO(GPIO).
DIO_NPN : DI/DO type.
1 : PNP (Source) mode for European rule;
0 : NPN (Sink) mode for Japanese rule.
Return :
TRUE (1) : Success.
FALSE (0) : Fail (Driver not exists, or version is too old, or machine not match).

BOOL get_IO1_configuration(BYTE *Iso, BYTE *DI_mode, BYTE *DO_mode, WORD *Mask)
BOOL get_IO2_configuration(BYTE *Iso, BYTE *DI_mode, BYTE *DO_mode, WORD *Mask)
Get DIO configuration (by variable)
Isolate_Type : DIO type.
1 : Isolated DIO;
0 : Non-Isolated DIO(GPIO).
DI_mode ([7:0]) : DI type, pin setting by hexadecimal bitmask only for Isolated DIO.
0xFF : PNP (Source) mode for European rule;
0 : NPN (Sink) mode for Japanese rule.
DO_mode : DO type only for Isolated DIO.
1 : PNP (Source) mode for European rule;
0 : NPN (Sink) mode for Japanese rule.
Mask ([15:0]): In/Out, pin setting by hexadecimal bitmask only for Non-Isolated DIO(GPIO).
1 : Output;
0 : Input
Return :
TRUE (1) : Success.
FALSE (0) : Fail (Initial error, or call by pointer error, or hardware problem).

BOOL set_IO1_configuration(BYTE Iso, BYTE DI_mode, BYTE DO_mode, WORD Mask)
BOOL set_IO2_configuration(BYTE Iso, BYTE DI_mode, BYTE DO_mode, WORD Mask)

Set DIO configuration.

Isolate_Type : DIO type.

1 : Isolated DIO;

0 : Non-Isolated DIO(GPIO).

DI_mode ([7:0]) : DI type, pin setting by hexadecimal bitmask only for Isolated DIO.

0xFF : PNP (Source) mode for European rule;

0 : NPN (Sink) mode for Japanese rule.

DO_mode : DO type only for Isolated DIO.

1 : PNP (Source) mode for European rule;

0 : NPN (Sink) mode for Japanese rule.

Mask ([15:0]) : In/Out, pin setting by hexadecimal bitmask only for Non-Isolated DIO(GPIO).

1 : Output;

0 : Input

Return :

TRUE (1) : Success.

FALSE (0) : Fail (Initial error or hardware problem).

BOOL get_DIO1(BYTE *DO_data, BYTE *DI_data)
BOOL get_DIO2(BYTE *DO_data, BYTE *DI_data)

Get isolated DIO output(DO) and input (DI).

DI ([7:0]) : Input state, pin setting by hexadecimal bitmask.

1 : High;

0 : Low.

DO ([7:0]) : Output state, pin setting by hexadecimal bitmask.

1 : High;

0 : Low.

Return :

TRUE (1) : Success.

FALSE (0) : Fail (Initial error or hardware problem).

FALSE (0) : Fail (Initial error or hardware problem).

BOOL set_DIO1(BYTE DO_data)
BOOL set_DIO2(BYTE DO_data)

Set isolated DIO output(DO).

DO ([7:0]) : Output state, pin setting by hexadecimal bitmask.

1 : High;

0 : Low.

Return :

TRUE (1) : Success.

FALSE (0) : Fail (Initial error or hardware problem).

FALSE (0) : Fail (Initial error or hardware problem).

BOOL config_COMPORT(BYTE *PORT_NUM)

Set COMPORT configuration.

A. PORT_NUM : Usable COMPORT number.
Range : 1~6.

Return :

TRUE (1) : Success.

FALSE (0) : Fail (Initial error, or setup 0, or hardware problem).

BOOL set_COMPORT_mode(BYTE port, BYTE mode, BYTE term)

Set COMPORT mode.

B. port : which port set.
Range : 1~6.

C. mode : Usable COMPORT number.
0 : RS232 mode;
1 : RS422-5Wire mode.
2 : RS422-9Wire mode;
4 : RS485 mode.
4 : Loopback mode.

D. term : Termination enable for RS422/RS485 mode.
1 : Enable;
0 : Disable.

Return :

TRUE (1) : Success.

FALSE (0) : Fail (Initial error or hardware problem).

BOOL get_COMPORT_mode(BYTE port, BYTE *mode, BYTE term)

Get COMPORT mode.

E. port : which port get.
Range : 1~6.

F. mode : Usable COMPORT number.
0 : RS232 mode;
1 : RS422-5Wire mode.
2 : RS422-9Wire mode;
4 : RS485 mode.
4 : Loopback mode.

G. term : Termination enable for RS422/RS485 mode.
1 : Enable;
0 : Disable.

Return :

TRUE (1) : Success.

FALSE (0) : Fail (Initial error or hardware problem).

APPENDIX C : Power Consumption

Testing Board	ICS-2000
RAM	32GB * 6
USB-1	USB Micsoft Wired Keyboard 600
USB-2	USB Mouse HP G1K28AA
SATA 0	Transcend M.2 TS512GMTE460T 512GB
Graphics output	DP
Power plan	Balance(Windows Sever 2019 Power plan)
Power Source1	Chroma 62006P-100-25
Test Program-1	CPU-Z
Test Program-2	BurnIn Test

C.1 AMD EPYC™ 8224P (64M Cache, up to 3.00 GHz)

Power on and boot to Windows Sever 2019 64-bit (without turbo boost technology)

CPU	Power Input	Standby Mode		Power on and boot to Windows Sever 2019 64bit			
				idle status CPU usage		Run 100% CPU usage	
		Max Current	Max Consumption	Max Current	Max Consumption	Max Current	Max Consumption
EPYC™ 8224P	16V	7.781A	124.5W	7.812A	124.99W	11.041A	176.66W
EPYC™ 8224P	24V	5.309A	127.41W	5.334A	128.02W	7.781A	186.74W
EPYC™ 8224P	36V	3.681A	132.52W	3.717A	133.81W	5.321A	191.57W
EPYC™ 8224P	50V	2.674A	133.7W	2.681A	134.05W	3.891A	194.55W

D

APPENDIX D : Supported Memory and Storage List

D.1 Supported Memory List

Testing Board	ICS-2000
Memory Test	MemTest86 V11.0
BurnInTest	BurnInTest Pro V10.2 (Build 1006)

Tset Item

Channel	Memtest	Burn In	Reboot
DIMM1~DIMM6	PASS	PASS	PASS

D.2 Supported ECC Memory List

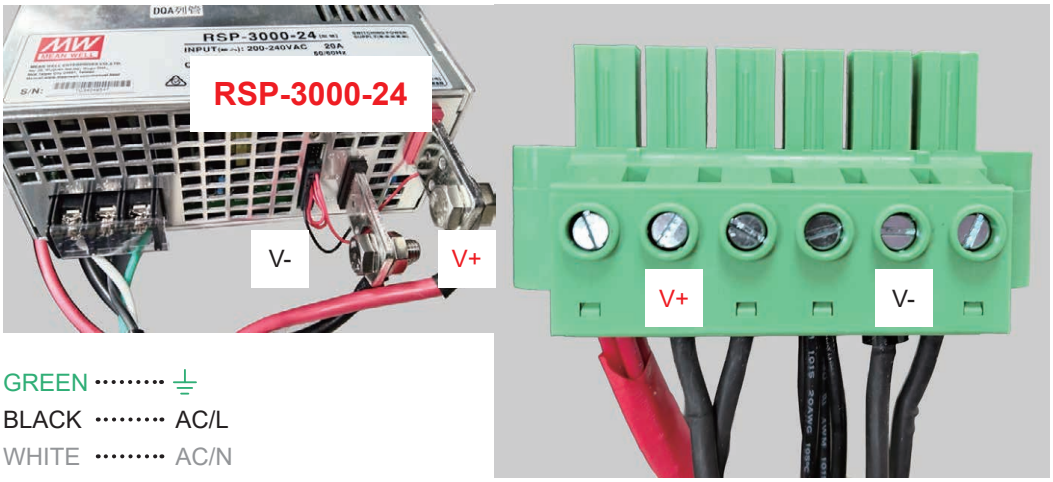
Brand	Info	Test
Innodisk 32G ECC DDR5-5600 R-DIMM	KSM48E40BD8KM-32HM	25ºC
TEAMGROUP 16G ECC DDR5-5600 R-DIMM	TE16GFREV2MH	25ºC

D.3 Supported Storage Device List

Type	Brand	Model	Capacity
U.2 PCIe SSD	Innodisk	4TG2-P DGEU2-08TDP1KCAEF-H03	8TB
M.2 PCIe SSD	Innodisk	4TG2-P DGM28-C12DP1KCAEF-H03 G4X4	512GB
		3TE6 DEM28-C12DD1KCCQF-H03 G3X2	512GB
	Transcend	TS512GMTE720T G4X4	512GB
		TS512GMTE460T G3X2	512GB

APPENDIX E : How to Install Power Supply

E.1 RSP-3000-24 Power Supply



GREEN ····· ⏚
BLACK ····· AC/L
WHITE ····· AC/N

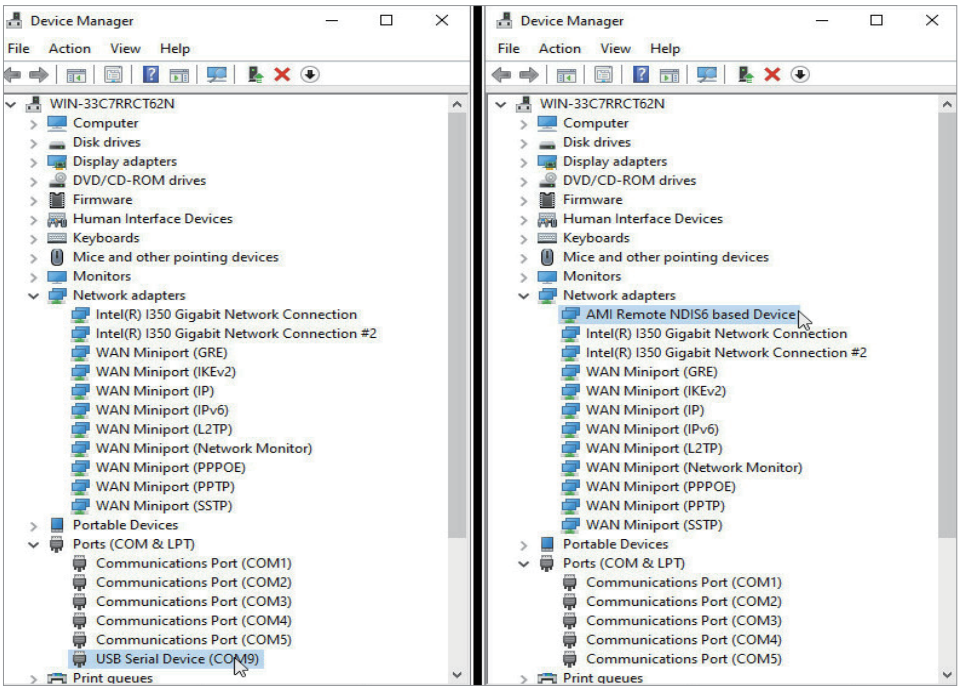
APPENDIX F : USB Over LAN Windows Driver Installation

The USB Over LAN driver supports Windows Server 2019 and Windows Server 2022.

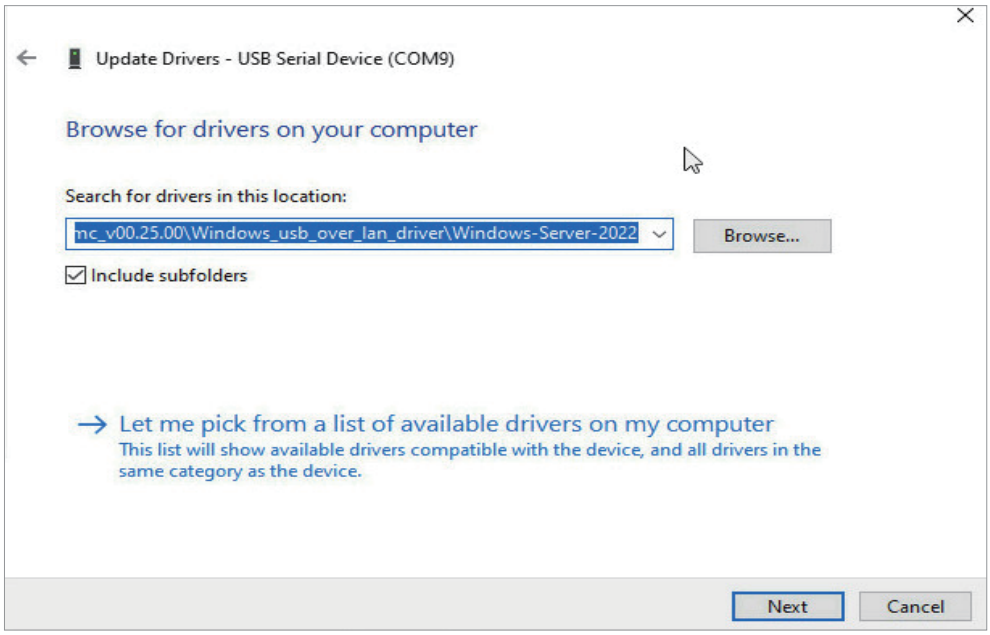
To enable USB Over LAN, the Power Saving Mode should be disabled.
Please use the following command to disable it.
Syntax
ipmitool raw 0x32 0xaa <action>
Parameters
<action>:
0 – Disable Power Saving Mode
1 – Enable Power Saving Mode

After Power Saving Mode is disabled, the USB Over LAN device will be recognized as a USB serial device, as shown in the figure below.

After updating its driver using the firmware release package, the device will appear as a network adapter.



Update the device driver by browsing to the path of the firmware release package, as shown below.





Note:
If failed to set the Power Saving Mode as below, please close the remote KVM console and try again.

ipmitool -I lanplus -H 192.168.10.11 -U vecow -P Vec0w@rz raw 0x32 0xaa 0
Unable to send RAW command (channel=0x0 netfn=0x32 lun=0x0 cmd=0xaa rsp=0xc0): Node busy

** If more help is needed, please contact Vecow Technical Support.

Vecow

For further support information, please visit www.vecow.com

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